Description

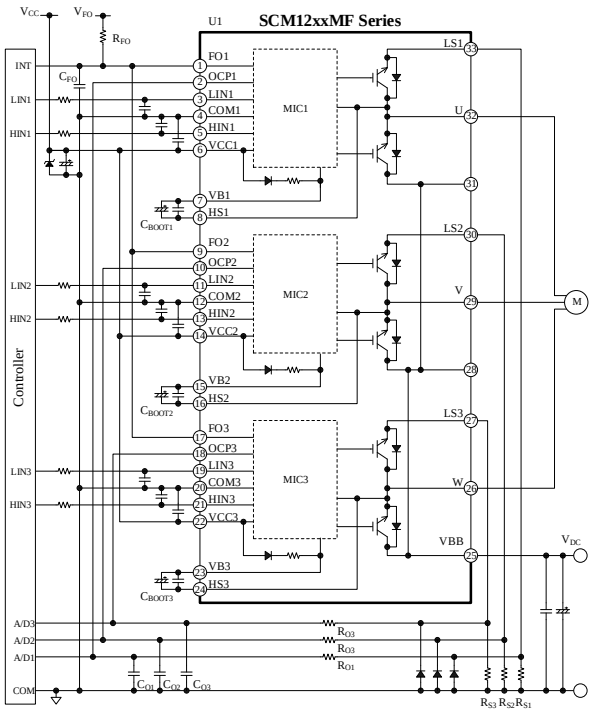
The SCM1200MF series are high voltage 3-phase motor driver ICs in which transistors, pre-driver ICs (MICs), and bootstrap circuits (diodes and resistors) are highly integrated.

These products can run on a 3-shunt current detection system and optimally control the inverter systems of medium-capacity motors that require universal input standards.

Features

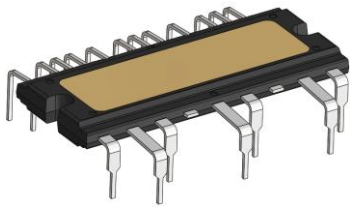
- Each Half-bridge Circuit Consists of a Pre-driver IC
- In Case of Abnormal Operation, All Outputs Shut Down via Three FO Pins Connected Together
- Built-in Bootstrap Diodes with Current Limiting Resistors (22 Ω)
- CMOS-compatible Input (3.3 V or 5 V)
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Isolation Voltage: 2500 V (for 1 min), UL-recognized Component (File No.: E118037)
- Fault Signal Output at Protection Activation
- Protections Include:
  Undervoltage Lockout for Power Supply
    High-side (UVLO_VB): Auto-restart
    Low-side (UVLO_VCC): Auto-restart
  Overcurrent Protection (OCP): Auto-restart
  Simultaneous On-state Prevention: Auto-restart
  Thermal Shutdown (TSD): Auto-restart

Typical Application



Package

DIP33
Pin Pitch: 1.27 mm
Mold Dimensions: 47 mm × 19 mm × 4.4 mm



Not to scale

Selection Guide

- Power Device: IGBT + FRD (600 V)

I_O	Feature	Part Number
10 A	Low noise	SCM1261MF*
15 A	Low noise	SCM1242MF
		SCM1263MF*
	Low switching dissipation	SCM1243MF
20 A	Low noise	SCM1265MF*
	Low switching dissipation	SCM1245MF
30 A	Low noise	SCM1256MF
	Low switching dissipation	SCM1246MF

* Uses a shorter blanking time for OCP activation.

Applications

For motor drives such as:

- Refrigerator Compressor Motor
- Air Conditioner Compressor Motor
- Washing Machine Main Motor
- Fan Motor
- Pump Motor

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25°C.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBB–LSx	450	V	
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBB–LSx	500	V	
IGBT Breakdown Voltage	V_{CES}	V_{CC} = 15 V, I_C = 1 mA, V_{IN} = 0 V	600	V	
Logic Supply Voltage	V_{CC}	VCCx–COMx	20	V	
	V_{BS}	VBx–HSx	20		
Output Current[1]	I_O	T_C = 25 °C, T_j < 150 °C	10	A	SCM1261MF
			15		SCM1242MF/63MF/43MF
			20		SCM1265MF/45MF
			30		SCM1256MF/46MF
Output Current (Pulse)	I_{OP}	T_C = 25 °C, $P_W \leq$ 1 ms, single pulse	20	A	SCM1261MF
			30		SCM1242MF/63MF/ 43MF/65MF/45MF
			45		SCM1256MF/46MF
Input Voltage	V_{IN}	HINx–COMx, LINx–COMx	−0.5 to 7	V	
FO Pin Voltage	V_{FO}	FOx–COMx	−0.5 to 7	V	
OCP Pin Voltage	V_{OCP}	OCPx–COMx	−10 to 5	V	
Operating Case Temperature[2]	$T_{C(OP)}$		−30 to 125	°C	
Junction Temperature[3]	T_j		150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	
Isolation Voltage[4]	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2500	V	

[1] Should be derated depending on an actual case temperature. See Section 15.4.
[2] Refers to a case temperature measured during IC operation.
[3] Refers to the junction temperature of each chip built in the IC, including the monolithic ICs (MICs), transistors, and freewheeling diodes.
[4] Refers to voltage conditions to be applied between the case and all pins. All pins have to be shorted.

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	COM1 = COM2 = COM3; VBB–COM	—	300	400	V	
Logic Supply Voltage	V_{CC}	VCCx–COMx	13.5	—	16.5	V	
	V_{BS}	VBx–HSx	13.5	—	16.5	V	
Input Voltage (HINx, LINx, FOx)	V_{IN}		0	—	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	µs	
	$t_{IN(MIN)OFF}$		0.5	—	—	µs	
Dead Time of Input Signal	t_{DEAD}		1.0	—	—	µs	SCM1243MF/ 45MF/46MF
			1.5	—	—		SCM1242MF/56MF/ 61MF/63MF/65MF
FO Pin Pull-up Resistor	R_{FO}		1	—	22	kΩ	
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V	
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	µF	
Bootstrap Capacitor	C_{BOOT}		10	—	220	µF	
Shunt Resistor	R_S	$I_P \leq 45$ A	12	—	—	mΩ	SCM1256MF/46MF
		$I_P \leq 30$ A	18	—	—		SCM1242MF/43MF/ 63MF/65MF/45MF
		$I_P \leq 20$ A	27	—	—		SCM1261MF
RC Filter Resistor	R_O		—	—	100	Ω	
RC Filter Capacitor	C_O		1000	—	2200	pF	SCM124xMF SCM125xMF
			1000	—	10000		SCM126xMF
PWM Carrier Frequency	f_C		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V.

3.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCCx–COMx	10.5	11.5	12.5	V	
	$V_{BS(ON)}$	VBx–HSx	10.5	11.5	12.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCCx–COMx	10.0	11.0	12.0	V	
	$V_{BS(OFF)}$	VBx–HSx	10.0	11.0	12.0	V	
Logic Supply Current	I_{CC}	VCC1 = VCC2 = VCC3, COM1 = COM2 = COM3; VCC pin current in 3-phase operation	—	3	—	mA	
	I_{BS}	VBx–HSx = 15 V, HINx = 5 V; VBx pin current in 1-phase operation	—	140	—	μA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, FOx)	V_{IH}		1.5	2.0	2.5	V	
Low Level Input Threshold Voltage (HINx, LINx, FOx)	V_{IL}		1.0	1.5	2.0	V	
High Level Input Current (HINx, LINx)	I_{IH}	V_{IN} = 5 V	—	230	500	μA	
Low Level Input Current (HINx, LINx)	I_{IL}	V_{IN} = 0 V	—	—	2	μA	
Fault Signal Output							
FO Pin Voltage at Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	—	—	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	—	—	V	
Protection							
OCP Threshold Voltage	V_{TRIP}		0.46	0.50	0.54	V	
OCP Hold Time	t_P		20	26	—	μs	
OCP Blanking Time	t_{BK}	V_{TRIP} = 1 V	—	1.65	—	μs	SCM124xMF SCM125xMF
			—	0.54	—		SCM126xMF
TSD Operating Temperature*	T_{DH}		135	150	—	°C	
TSD Releasing Temperature*	T_{DL}		105	120	—	°C	

* Refers to the junction temperature of the built-in monolithic ICs (MICs).

3.2. Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	10	μA	
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	1.1	1.3	V	
Bootstrap Diode Series Resistor	R_{BOOT}		17.6	22.0	26.4	Ω	

3.3. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance[1]	$R_{(j-c)Q}$[2]	1 element operating (IGBT)	—	—	3.7	°C/W	SCM1261MF
			—	—	3		SCM12/42MF/ 63MF/43MF/65MF/ 45MF/56MF/46MF
	$R_{(j-c)F}$[3]	1 element operating (freewheeling diode)	—	—	4.5	°C/W	SCM1261MF
			—	—	4		SCM12/42MF/ 63MF/43MF/65MF/ 45MF/56MF/46MF

[1] Refers to a case temperature at the measurement point described in Figure 3-1, below.
[2] Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 15.1.
[3] Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

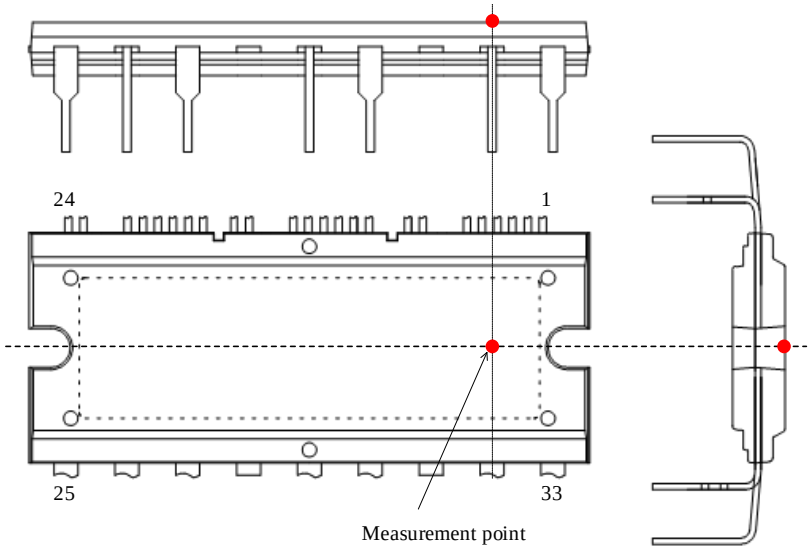


Figure 3-1. Case Temperature Measurement Point

3.4. Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections.

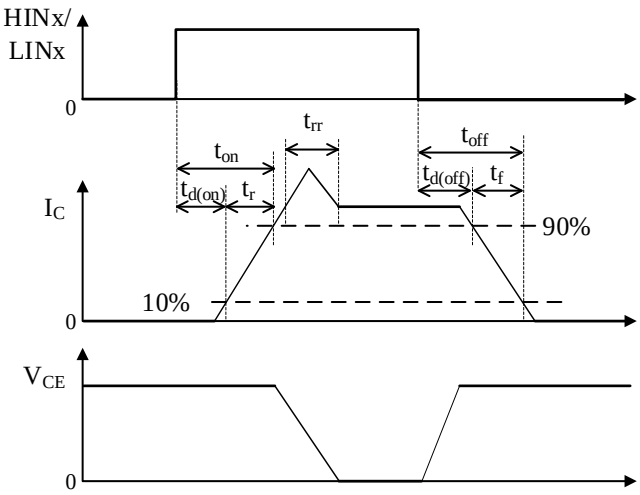


Figure 3-2. Switching Characteristics Definitions

3.4.1. SCM1261MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 10 A, V_{IN} = 0 V	—	1.7	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 10 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	85	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1070	—	ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 10 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	105	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	710	—	ns
Rise Time	t_r		—	120	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1010	—	ns
Fall Time	t_f		—	95	—	ns

3.4.2. SCM1242MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 15 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 15 A, V_{IN} = 0 V	—	1.75	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1300	—	ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	90	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1230	—	ns
Fall Time	t_f		—	90	—	ns

3.4.3. SCM1263MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 15 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 15 A, V_{IN} = 0 V	—	1.75	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1300	—	ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	90	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1230	—	ns
Fall Time	t_f		—	90	—	ns

3.4.4. SCM1243MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 15 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 15 A, V_{IN} = 0 V	—	1.75	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	70	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	600	—	ns
Rise Time	t_r		—	70	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	620	—	ns
Fall Time	t_f		—	60	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	600	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	600	—	ns
Fall Time	t_f		—	70	—	ns

3.4.5. SCM1265MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 20 A, V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	780	—	ns
Rise Time	t_r		—	120	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1150	—	ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	85	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	810	—	ns
Rise Time	t_r		—	170	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1100	—	ns
Fall Time	t_f		—	90	—	ns

3.4.6. SCM1245MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 20 A, V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	75	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	695	—	ns
Rise Time	t_r		—	95	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	675	—	ns
Fall Time	t_f		—	55	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	115	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	715	—	ns
Rise Time	t_r		—	135	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	670	—	ns
Fall Time	t_f		—	50	—	ns

3.4.7. SCM1256MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 30 A, V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	70	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	760	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1260	—	ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	770	—	ns
Rise Time	t_r		—	160	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1200	—	ns
Fall Time	t_f		—	90	—	ns

3.4.8. SCM1246MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 30 A, V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	60	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	660	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	700	—	ns
Fall Time	t_f		—	50	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	70	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	660	—	ns
Rise Time	t_r		—	150	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	690	—	ns
Fall Time	t_f		—	50	—	ns

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	*	0.588	—	0.784	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	200	μm	
Package Weight		—	11.8	—	g	

* When mounting a heatsink, it is recommended to use a metric screw of M3 and a plain washer of 7 mm (φ) together at each end of it. For more details about screw tightening, see Section 13.2.

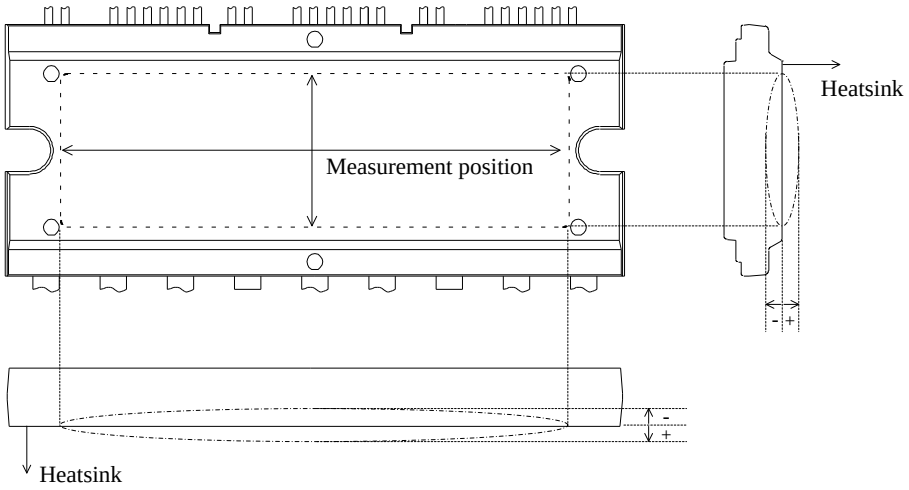


Figure 4-1. Flatness Measurement Position

5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	2.0	—	2.5	mm	
Creepage		3.86	—	4.26	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

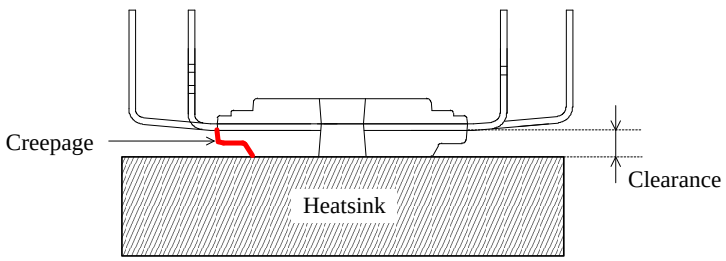


Figure 5-1. Insulation Distance Definitions

6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HIxN and LINx signals in each phase are high at the same time, the simultaneous on-state prevention sets both the high- and low-side transistors off.

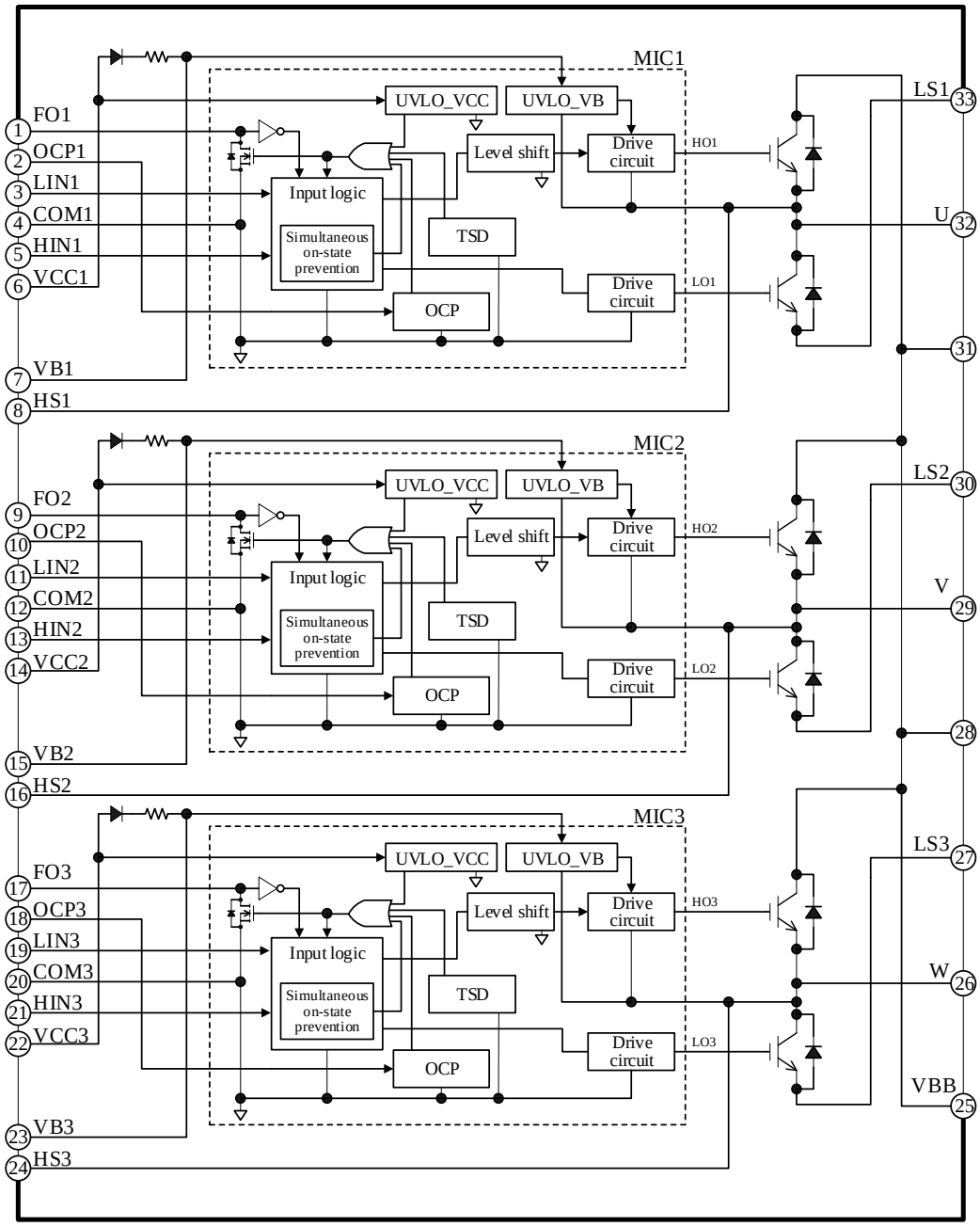
After the IC recovers from a UVLO_VCC condition, the high- and low-side transistors resume switching, according to the input logic levels of the HINx and LINx signals (level-triggered).

After the IC recovers from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

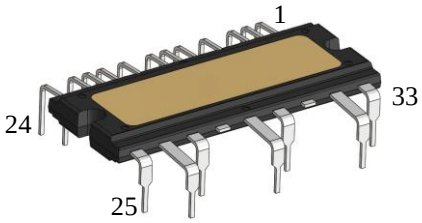
Table 6-1. Truth Table for Operation Modes

Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
External Shutdown Signal Input FO = L	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Undervoltage Lockout for High-side Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Thermal Shutdown (TSD)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF

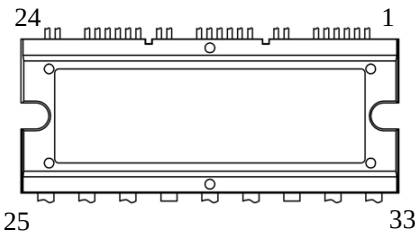
7. Block Diagram



8. Pin Configuration Definitions



Top view



Pin Number	Pin Name	Description
1	FO1	U-phase fault output and shutdown signal input
2	OCP1	Input for U-phase overcurrent protection
3	LIN1	Logic input for U-phase low-side gate driver
4	COM1	U-phase logic ground
5	HIN1	Logic input for U-phase high-side gate driver
6	VCC1	U-phase logic supply voltage input
7	VB1	U-phase high-side floating supply voltage input
8	HS1	U-phase high-side floating supply ground
9	FO2	V-phase fault output and shutdown signal input
10	OCP2	Input for V-phase overcurrent protection
11	LIN2	Logic input for V-phase low-side gate driver
12	COM2	V-phase logic ground
13	HIN2	Logic input for V-phase high-side gate driver
14	VCC2	V-phase logic supply voltage input
15	VB2	V-phase high-side floating supply voltage input
16	HS2	V-phase high-side floating supply ground
17	FO3	W-phase fault output and shutdown signal input
18	OCP3	Input for W-phase overcurrent protection
19	LIN3	Logic input for W-phase low-side gate driver
20	COM3	W-phase logic ground
21	HIN3	Logic input for W-phase high-side gate driver
22	VCC3	W-phase logic supply voltage input
23	VB3	W-phase high-side floating supply voltage input
24	HS3	W-phase high-side floating supply ground
25	VBB	Positive DC bus supply voltage
26	W	W-phase output
27	LS3	W-phase IGBT emitter
28	VBB	(Pin trimmed) positive DC bus supply voltage
29	V	V-phase output
30	LS2	V-phase IGBT emitter
31	VBB	(Pin trimmed) positive DC bus supply voltage
32	U	U-phase output
33	LS1	U-phase IGBT emitter

9. Typical Applications

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

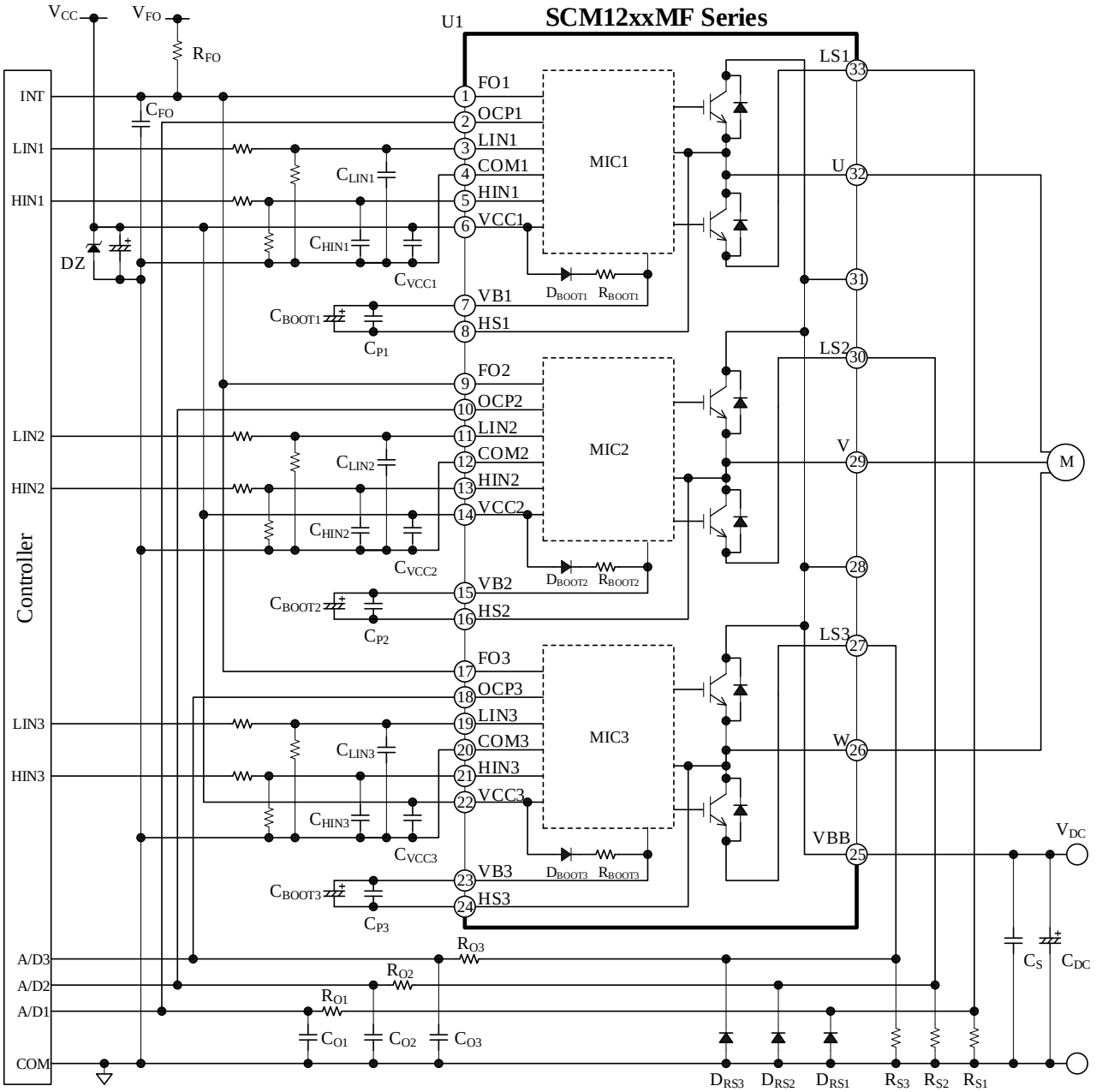


Figure 9-1. Typical Application Using Three Shunt Resistors

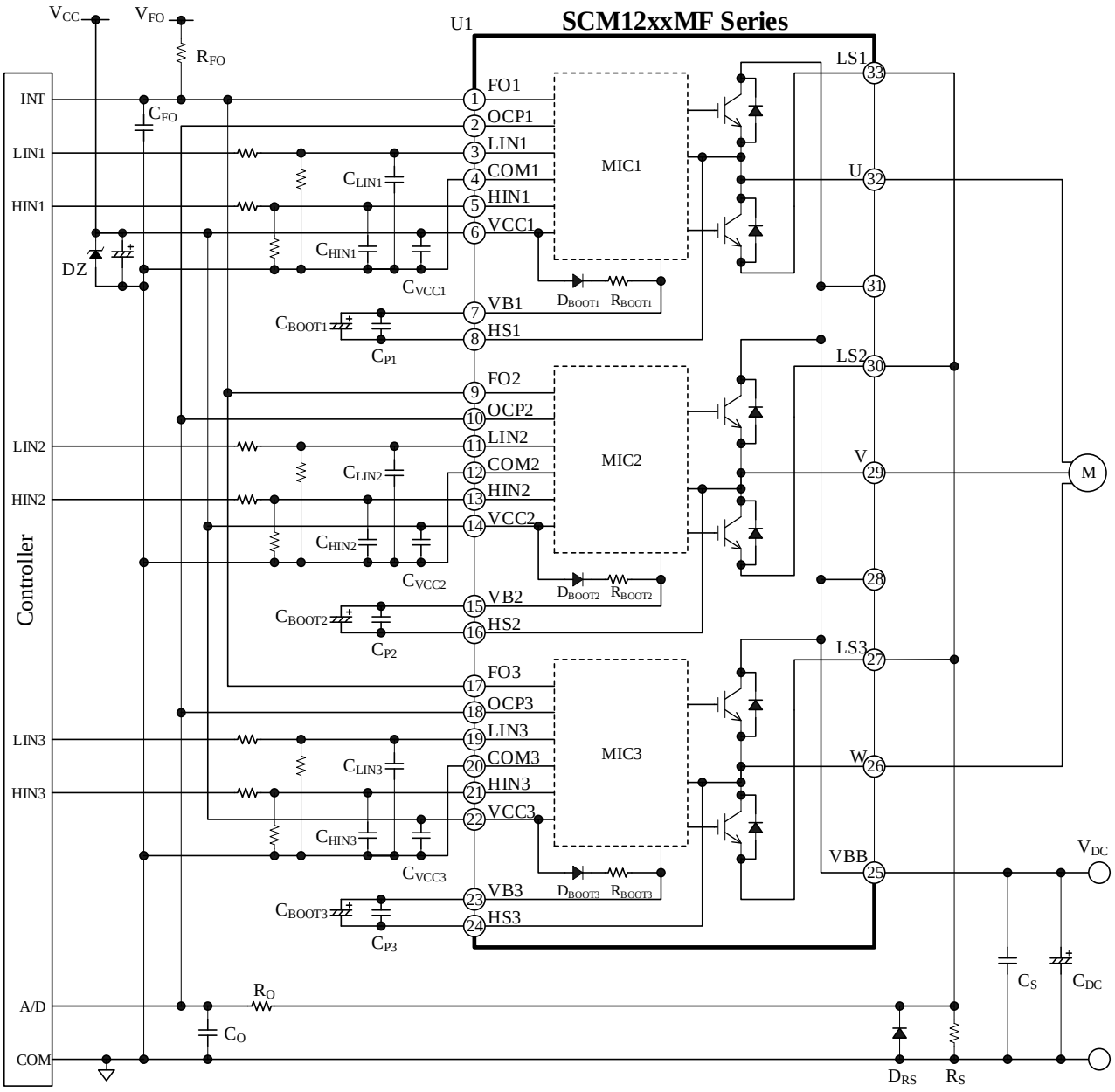
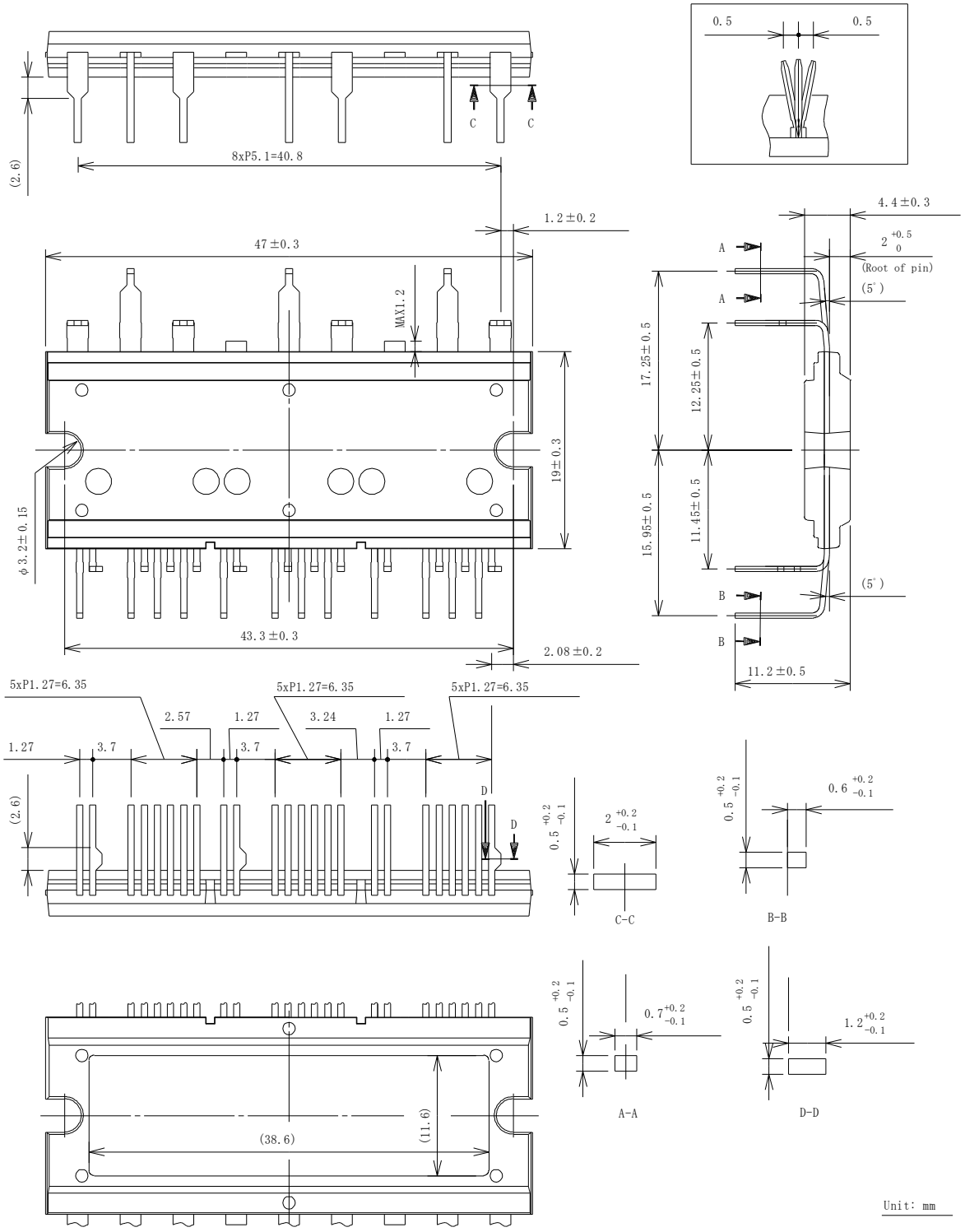


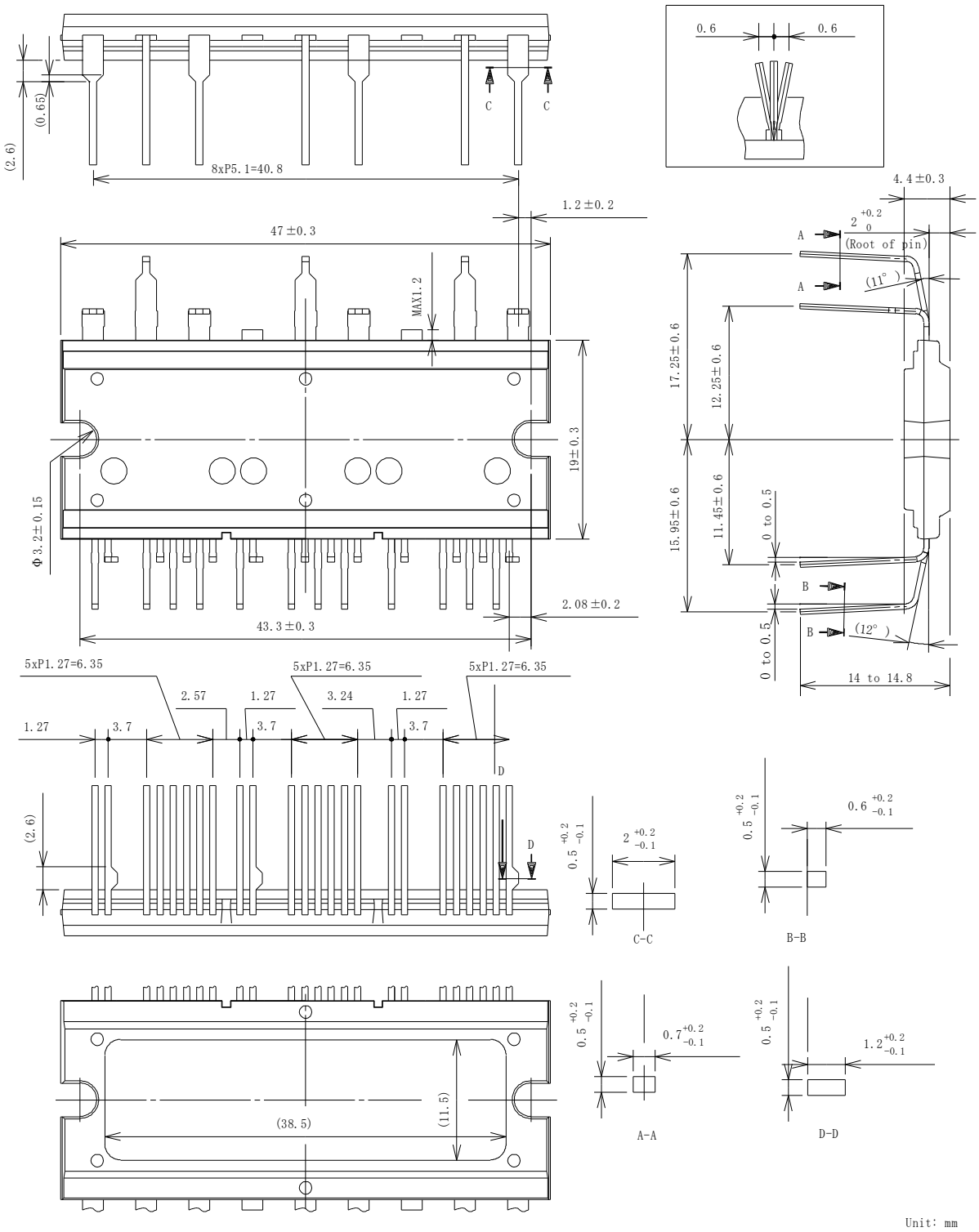
Figure 9-2. Typical Application Using a Single Shunt Resistor

10. Physical Dimensions

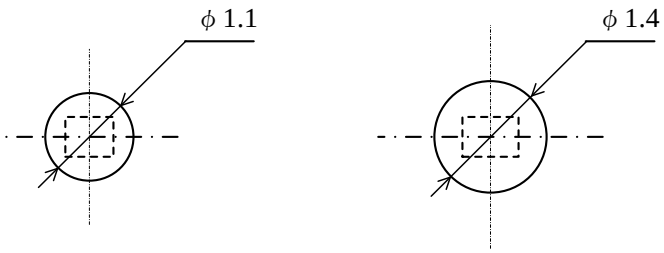
10.1. Leadform 2552



10.2. Leadform 2557 (Long Lead Type)

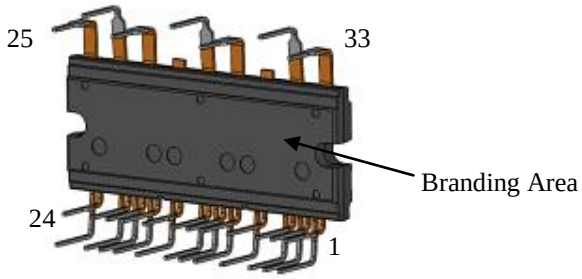


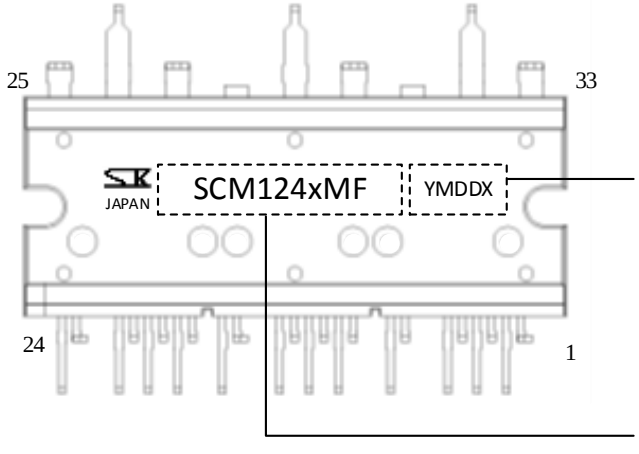
10.3. Reference PCB Hole Sizes



Pins 1 to 24 Pins 25 to 33

11. Marking Diagram





12. Functional Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

For pin descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. The U-, V-, and W-phases are represented as the pin numbers 1, 2, and 3, respectively. Thus, "the VBx pin" is used when referring to any or all of the VB1, VB2, or VB3 pin. Also, when different pin names are mentioned as a pair (e.g., "the VBx and HSx pins"), they are meant to be the pins in the same phase.

12.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences.

To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 12.5$ V). It is required to charge bootstrap capacitors, C_{BOOT}, up to full capacity at startup (see Section 12.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

12.2. Pin Descriptions

12.2.1. U, V, and W

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor.

The U, V, and W pins are internally connected to the HS1, HS2, and HS3 pins, respectively.

12.2.2. VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin.

Voltages between the VBB and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

12.2.3. VB1, VB2, and VB3

These are the inputs of the high-side floating power supplies for the individual phases.

Voltages across the VBx and HSx pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

In each phase, a bootstrap capacitor, C_{BOOTx}, should be connected between the VBx and HSx pins.

For proper startup, turn on the low-side transistor first, then charge the bootstrap capacitor, C_{BOOTx}, up to its maximum capacity.

For capacitance of the bootstrap capacitors, C_{BOOTx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{BOOTx}.

$$C_{BOOTx}\ (\mu F) > 800 \times t_{L(OFF)}\ (s) \quad (1)$$

$$10\ \mu F \leq C_{BOOTx} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Even during the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 12.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 12.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 12-1 shows, in each trace between the VCCx and VBx pins, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are placed in series.

Time constant for the charging time of C_{BOOTx}, τ, can be computed by Equation (3):

$$\tau = C_{BOOTx} \times R_{BOOTx}\ , \quad (3)$$

where C_{BOOTx} is the optimized capacitance of the bootstrap capacitor, and R_{BOOTx} is the resistance of the current-limiting resistor (22 Ω ± 20%).

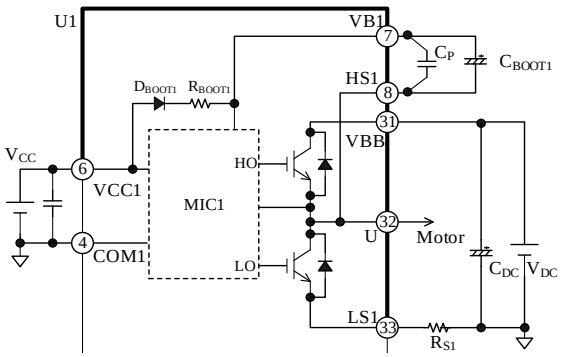


Figure 12-1. Bootstrap Circuit

Figure 12-2 shows an internal level-shifting circuit that produces high-side output signals, HOx. A high-side output signal, HOx, is generated accroding to an input signal, on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a "Set" signal is generated. When the HINx input singnal transits from high to low (falling edge), a "Reset" signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 12-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and HSx pins ("VBx–HSx") occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of the high-side output, HOx, stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high, the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition which may result in critical damage to the IC. To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC, and be connected between the VBx and HSx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_{Px}, in parallel near these pins used for the same phase.

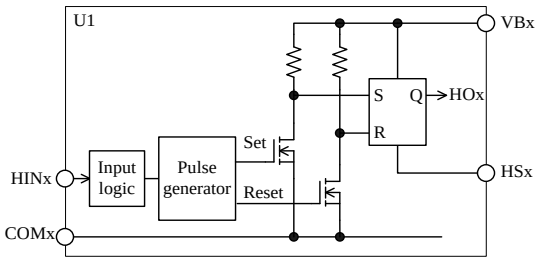


Figure 12-2. Internal Level-shifting Circuit

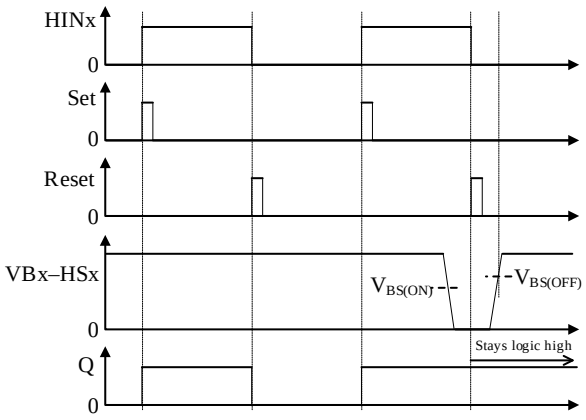


Figure 12-3. Waveforms at VBx–HSx Voltage Drop

12.2.4. HS1, HS2, and HS3

These pins are the grounds of the high-side floating power supplies for each phase, and are connected to the negative nodes of bootstrap capacitors, C_{BOOTx}.

The HS1, HS2, and HS3 pins are internally connected to the U, V, and W pins, respectively.

12.2.5. VCC1, VCC2, and VCC3

These are the logic supply pins for the built-in pre-driver ICs. The VCC1, VCC2, and VCC3 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{VCCx}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

12.2.6. COM1, COM2, and COM3

These are the logic ground pins for the built-in pre-driver ICs. For proper control, the control parts in each phase must be connected to the corresponding ground pin. The COM1, COM2, and COM3 pins should be connected externally on a PCB because they are not internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to shunt resistors, R_{Sx}, at a single-point ground (or star ground) which is separated from the power ground (see Figure 12-4).

Moreover, extreme care should be taken when wiring so that currents from the power ground do not affect the COMx pin.

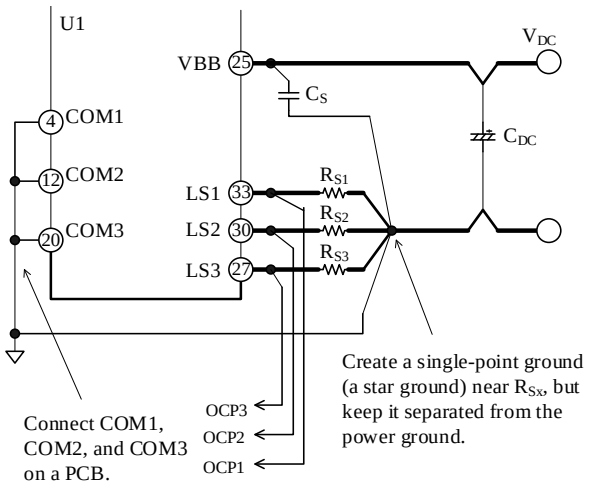


Figure 12-4. Connections to Logic Ground

12.2.7. HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller.

Figure 12-5 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 22 kΩ pull-down resistor, and its input logic is active high. Input signals applied across the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 12-1, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance.

Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 12-6).

Here are filter circuit constants for reference:

- R_{IN1x}: 33 Ω to 100 Ω
- R_{IN2x}: 1 kΩ to 10 kΩ
- C_{INx}: 100 pF to 1000 pF

Extra attention should be paid when adding R_{IN1x} and R_{IN2x} to the traces. When they are connected each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 12-1. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.0 µs (SCM1243MF/45MF/46MF) ≥1.5 µs (SCM1242MF/56MF/61MF/63MF/65MF)	

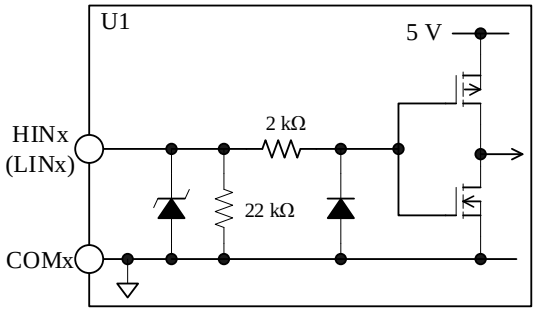


Figure 12-5. Internal Circuit Diagram of HINx or LINx Pin

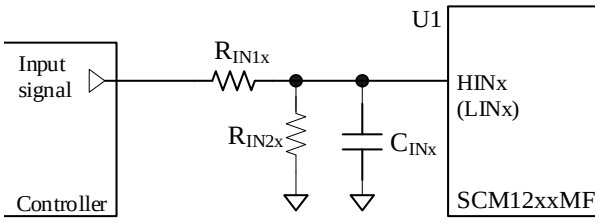


Figure 12-6. Filter Circuit for HINx or LINx Pin

12.2.8. LS1, LS2, and LS3

These are the emitter pins of the low-side IGBTs. For current detection, the LS1, LS2, and LS3 pins should be connected externally on a PCB via shunt resistors, R_{Sx}, to the COMx pins.

When connecting a shunt resistor, place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RSx}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

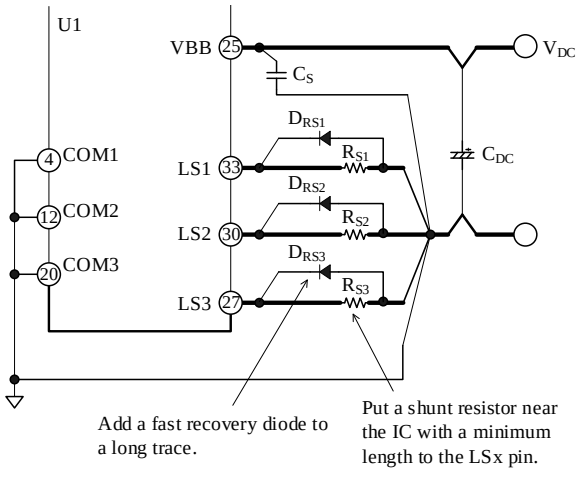


Figure 12-7. Connections to LSx Pin

12.2.9. OCP1, OCP2, and OCP3

These pins serve as the inputs of the overcurrent protection (OCP) for monitoring the currents going through the output transistors.

Section 12.3.4 provides further information about the OCP circuit configuration and its mechanism.

12.2.10. FO1, FO2, and FO3

These pins operate as the fault outputs and shutdown inputs for each phase. Sections 12.3.1 and 0 explain the two functions in detail, respectively.

Figure 12-8 illustrates a schematic diagram of the FOx pin and its peripheral circuit. Because of its open-drain nature, each of the FOx pins should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage (i.e., the FO Pin Pull-up Voltage, V_{FO}) should range from 3.0 V to 5.5 V.

Figure 12-10 shows a relation between the FOx pin voltage and the pull-up resistor, R_{FO}. When the pull-up resistor, R_{FO}, has a too small resistance, the FOx pin voltage at fault output becomes high due to the on-resistance of a built-in MOSFET, Q_{FO} (Figure 12-8). Therefore, it is recommended to use a 1 kΩ to 22 kΩ pull-up resistor when the Low Level Input Threshold Voltage of the microcontroller, V_{IL}, is set to 1.0 V.

To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FOx and COMx pins. Note that, however, this additional filtering allows a delay time, $t_{D(FO)}$, to occur, as seen in Figure 12-9. The delay time, $t_{D(FO)}$, is a period of time which starts when the IC receives a fault flag turning on the internal MOSFET, Q_{FO}, and continues until when the FOx pin reaches its threshold voltage (V_{IL}) of 1.0 V or below (put simply, until the time when the IC detects a logic low state, "L").

Figure 12-11 shows how the delay time, $t_{D(FO)}$, and the noise filter capacitor, C_{FO}, are related.

To avoid the repetition of OCP activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P, which occurs after the internal MOSFET (Q_{FO}) turn-on. t_P is 15 µs where minimum values of thermal characteristics are taken into account. (For more details, see Section 12.3.4.)

When V_{IL} is set to 1.0 V, it is recommended to use a 0.001 µF to 0.01 µF noise filter capacitor, C_{FO}, allowing a sufficient margin to deal with variations in characteristics.

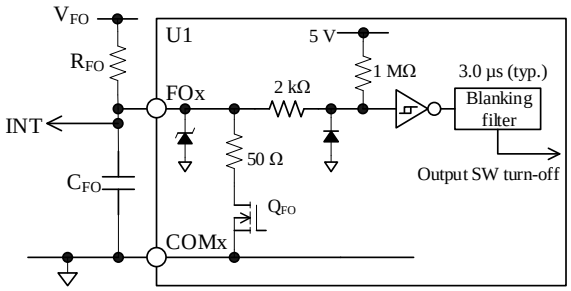


Figure 12-8. Internal Circuit Diagram of FOx Pin and Its Peripheral Circuit

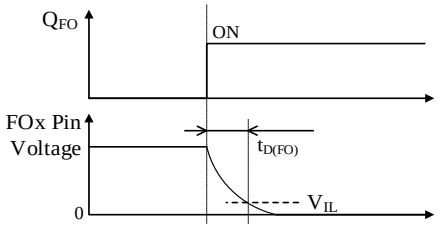


Figure 12-9. FOx Pin Delay Time, $t_{D(FO)}$

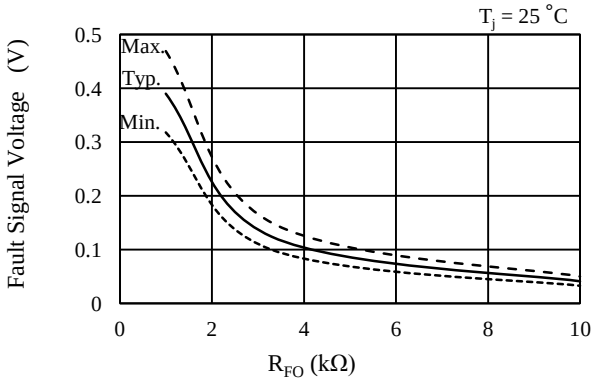


Figure 12-10. Fault Signal Voltage vs. Pull-up Resistor, R_{FO}

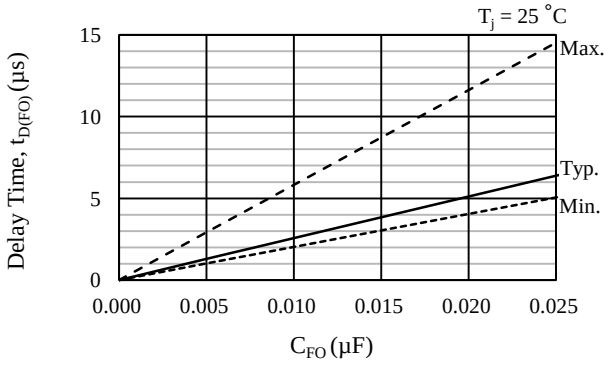


Figure 12-11. Delay Time, $t_{D(FO)}$ vs. Filter Capacitor, C_{FO}

12.3. Protection Functions

This section describes the various protection circuits provided in the SCM1200MF series. The protection circuits include the undervoltage lockout for power supplies (UVLO), the simultaneous on-state prevention, the overcurrent protection (OCP), and the thermal shutdown (TSD). In case one or more of these protection circuits are activated, the FOx pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. The external microcontroller can also shut down the IC operations by inputting a fault signal to the FOx pin. In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor (see also the diagrams in Section 7). "VBx–HSx" refers to the voltages between the VBx and HSx pins.

12.3.1. Fault Signal Output

In case one or more of the following protections are actuated, an internal MOSFET, Q_{FO}, turns on, then the FOx pin becomes logic low (≤0.5 V).

1) Low-side undervoltage lockout (UVLO_VCC)
2) Overcurrent protection (OCP)
3) Simultaneous on-state prevention
4) Thermal shutdown (TSD)

During the time when the FOx pin holds the logic low state, the high- and low-side transistors of each phase turn off. In normal operation, the FOx pin holds a logic high state and outputs a 5 V signal.

The fault signal output time of the FOx pin at OCP activation is the OCP hold time (t_P) of 26 µs (typ.), fixed by a built-in feature of the IC itself (see Section 12.3.4). The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined OCP hold time, t_P.

12.3.2. Shutdown Signal Input

The FO1, FO2, and FO3 pins also can be the input pins of shutdown signals. When the FOx pin becomes logic low, the high- and low-side transistors of each phase turn off. The voltages and pulse widths of the shutdown signals to be applied between the FOx and COMx pins are listed in Table 12-2.

Table 12-2. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥3.0 µs	≥3.0 µs

In Figure 12-12, FO1, FO2 and FO3 are all connected. If an abnormal condition is detected by any one of the monolithic ICs (MICx), the high- and low-side transistors of all phases turn off at once.

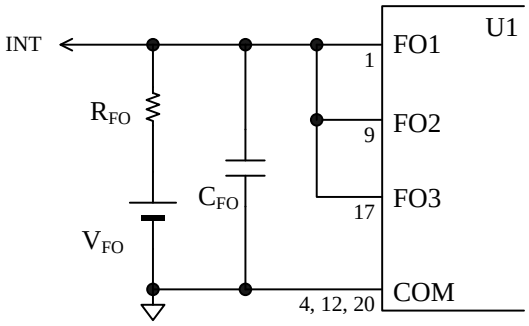


Figure 12-12. All-phase Shutdown Circuit

12.3.3. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SCM1200MF series has the undervoltage lockout (UVLO) circuits for both of the high- and low-side power supplies in each monolithic IC (MICx).

12.3.3.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 12-13 shows operational waveforms of the undervoltage lockout operation for high-side power supply (i.e., UVLO_VB).

When the voltage between the VBx and HSx pins (VBx–HSx) decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$, 11.0 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets only an HOx signal to logic low. When the voltage between the VBx and HSx pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$, 11.5 V) or more, the IC releases the UVLO_VB condition. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release.

The FOx pin does not transmit any fault signals during the UVLO_VB is in operation. In addition, the VBx pin has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

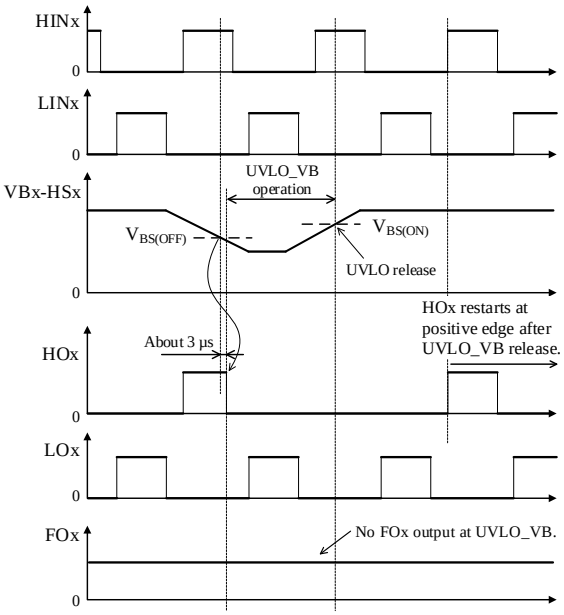


Figure 12-13. UVLO_VB Operational Waveforms

12.3.3.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 12-14 shows operational waveforms of the undervoltage lockout operation for low-side power supply (i.e., UVLO_VCC).

When the VCCx pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$, 11.0 V) or less, the UVLO_VCC circuit in the corresponding phase gets activated and sets both of HOx and LOx signals to logic low. When the VCCx pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$, 11.5 V) or more, the IC releases the UVLO_VCC condition. Then it resumes transmitting the HOx and LOx signals according to input commands on the HINx and LINx pins.

During the UVLO_VCC operation, the FOx pin becomes logic low and sends fault signals. In addition, the VCCx pin has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

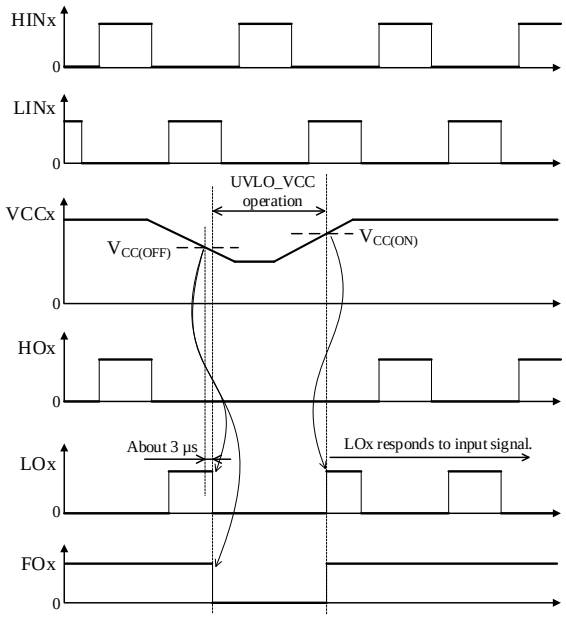


Figure 12-14. UVLO_VCC Operational Waveforms

12.3.4. Overcurrent Protection (OCP)

Figure 12-15 is an internal circuit diagram describing the OCPx pin and its peripheral circuit.

The OCPx pin detects overcurrents with the input voltages across external shunt resistors, R_{Sx}. Becuase the OCPx pin is internally pulled down, the OCPx pin voltage increases proportionally to a rise in the currents running through the shunt resistors, R_{Sx}.

Figure 12-16 is a timing chart that represents operation waveforms during OCP operation. When the OCPx pin voltage increases to the OCP Threshold Voltage (V_{TRIP}, 0.50 V) or more, and remains in this condition for a period of the OCP Blanking Time (t_{BK}, 1.65 µs) or longer, the OCPx circuit is activated. The enabled OCPx circuit shuts off the output transistors and puts the FOx pin into a logic low state. Then, output current decreases as a result of the output transistors turn-off. Even if the OCPx pin voltage falls below V_{TRIP}, the IC holds the FOx pin in the logic low state for a fixed OCP hold time (t_P) of 26 µs (typ.). Then, the output transistors operate according to input signals.

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected.

Care should also be taken when using a 3-shunt resistor system in your application. The IC running on the 3-shunt resistor system only shuts off the output transistor in the phase where an overcurrent condition

exists. And a fault signal is transmitted from the FOx pin of the phase being under the overcurrent condition.

As already shown in Figure 12-12, if all of the FOx pins being used makes a short circuit, a fault signal sent from the corresponding phase can turn off the output transistors of all phases (see Section 0).

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_{Sx} (see Section 2).
- Set the OCPx pin input voltage to vary within the rated OCP pin voltages, V_{OCP} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistors, R_{Sx}. In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor, R_O, and a filter capacitor, C_O) to the OCPx pin, care should be taken in setting the time constants of R_O and C_O. The larger the time constant, the longer the time that the OCPx pin voltage rises to V_{TRIP}. And this may cause permanent damage to the transistors. Consequently, a propagation delay of the IC must be taken into account when you determine the time constants. For R_O and C_O, their time constants must be set to the values listed in Table 12-3.

The filter capacitor, C_O, should also be placed near the IC, between the OCPx and COMx pins with a minimal length of traces.

Note that overcurrents are undetectable when one or more of the U, V, and W pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

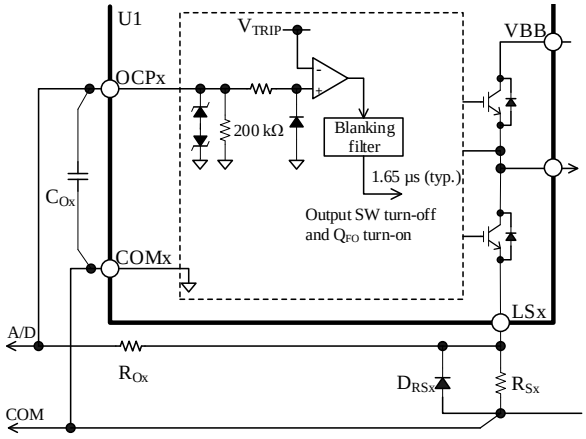


Figure 12-15. Internal Circuit Diagram of OCPx Pin and Its Peripheral Circuit

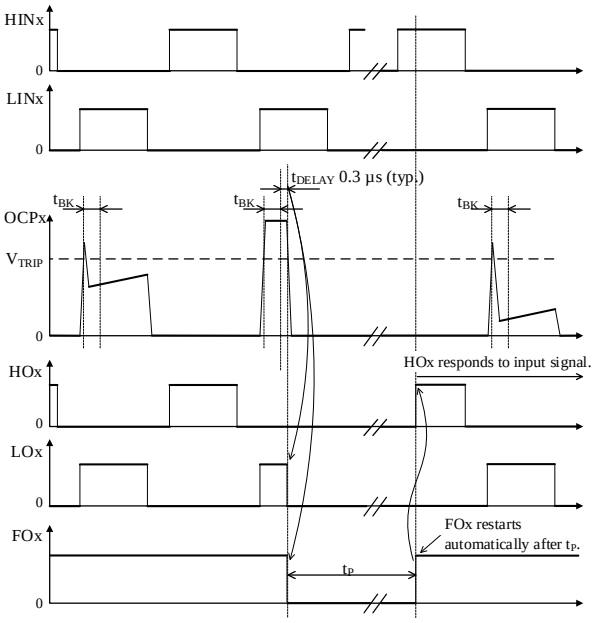


Figure 12-16. OCP Operational Waveforms

Table 12-3. Reference Time Constants for CR Filter

Part Number	Time Constant (µs)
SCM124xMF SCM125xMF	≤0.22
SCM126xMF	≤1

12.3.5. Simultaneous On-state Prevention

In case both of the HINx and LINx pins receive logic high signals at once, the high- and low-side transistors turn on at the same time, causing overcurrents to pass through. As a result, the switching transistors will be destroyed. To prevent this event, the simultaneous on-state prevention circuit is built into each of the monolithic ICs (MICx). Note that incorrect command input and noise interference are also largely responsible for such a simultaneous-on condition.

When logic high signals are asserted on the HINx and LINx pins at once, as in Figure 12-17, this function gets activated and turns the high- and low-side transistors off. Then, during the function is being enabled, the FOx pin becomes logic low and sends fault signals. After the IC comes out of the simultaneous on-state condition, "HOx" and "LOx" start responding in accordance with HINx and LINx input commands again.

To prevent noise-induced malfunctions, the simultaneous on-state prevention circuit has a filter of about 0.8 µs.

Note that the function does not have any of dead-time programming circuits. Therefore, input signals to the HINx and LIN pins must have proper dead times as defined in Section 12.2.7.

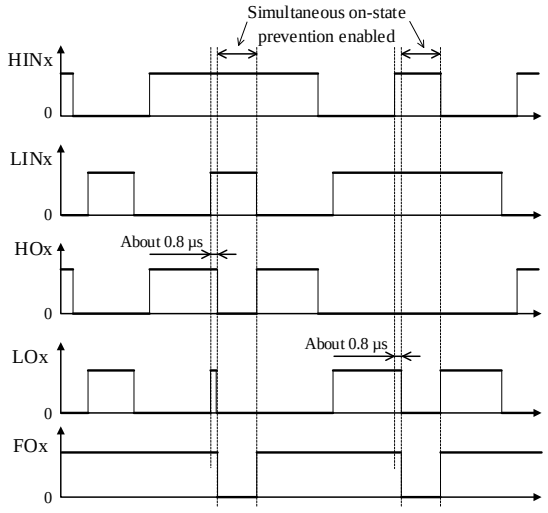


Figure 12-17. Operational Waveforms of Simultaneous On-state Prevention

12.3.6. Thermal Shutdown (TSD)

The SCM1200MF series incorporates a thermal shutdown (TSD) circuit in each phase. Figure 12-18 shows TSD operational waveforms.

In case of overheating (e.g., increased power dissipation due to overload, a rise in ambient temperature rise at the device, etc.), the IC shuts down the high- and low-side output transistors.

The TSD circuit in each monolithic IC (MICx) monitors temperatures (see Section 7).

When the temperature of the monolithic IC (MICx) exceeds the TSD Operating Temperature (T_{DH}, 150 °C), the corresponding TSD circuit is activated. When the temperature of the monolithic IC (MICx) decreases to the TSD Releasing Temperature (T_{DL}, 120 °C) or less, the shutdown condition is released. The transistors then resume operating according to input signals.

During the TSD operation, the FOx pin becomes logic low and transmits fault signals.

Note that junction temperatures of the output transistors themselves are not monitored; Therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

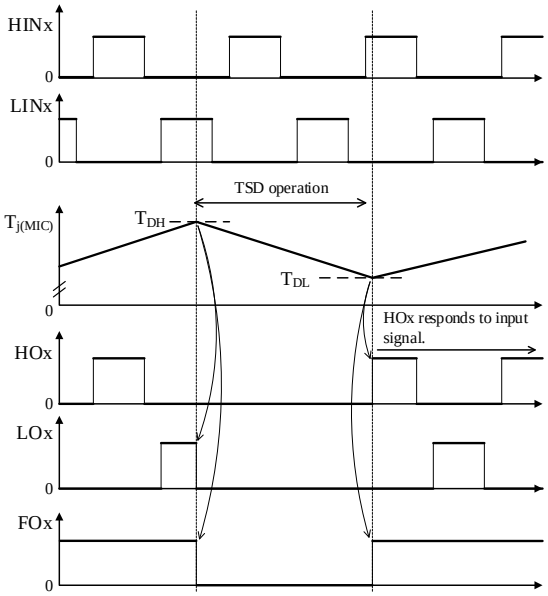


Figure 12-18. TSD Operational Waveforms

13. Design Notes

This section also employs the notation system described in the beginning of the previous section.

13.1. PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths carrying high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation.

Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which carry high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state.

In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

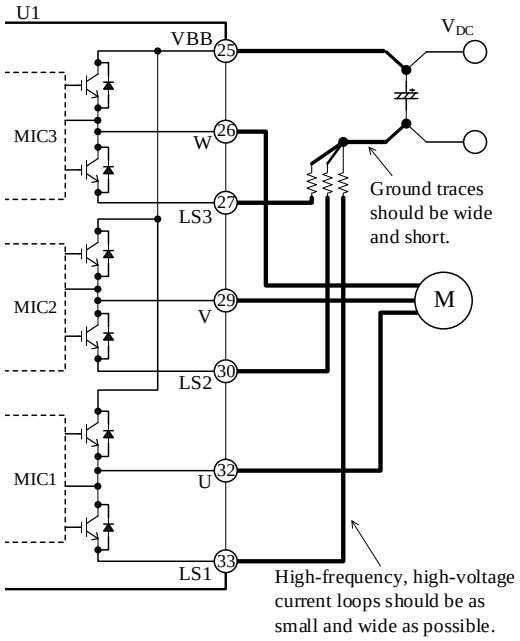


Figure 13-1. High-frequency, High-voltage Current Paths

13.2. Considerations in Heatsink Mounting

The following are the key considerations and guidelines for mounting a heatsink:

- It is recommended to use a pair of a metric screw of M3 and a plain washer of 7 mm (φ).
  To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 4.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there must be no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  – Grease thickness: 100 µm
  – Heatsink flatness: ±100 µm
  – Apply a silicone grease within the area indicated in Figure 13-2, below.

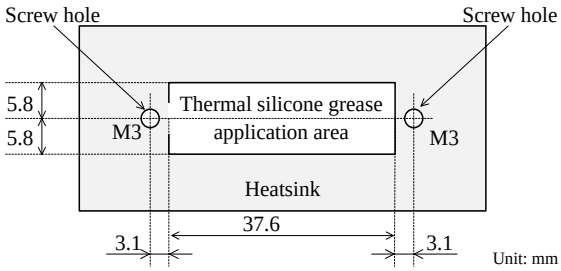


Figure 13-2. Reference Application Area for Thermal Silicone Grease

13.3. Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and emitter of each transistor should have the same potential.

Moreover, care should be taken when performing the measurements, because the collectors of the high-side transistors are all internally connected to the VBB pin.

The output (U, V, and W) pins are connected to the emitters of the corresponding high-side transistors, whereas the LSx pins are connected to the emitters of the low-side transistors. The gates of the high-side transistors are pulled down to the corresponding output (U, V, and W) pins; similarly, the gates of the low-side transistors are pulled down to the COMx pins.

Note that the output, LSx, and COMx pins must be connected appropriately before measuring breakdown voltage or leak current. Otherwise the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 13-3 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 13-4 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open.

Before conducting a measurement, be sure to isolate the ground of the to-be-measured phase from those of other two phases not to be measured. Then, in each of the two phases, which are separated not to be measured, connect the LSx and COMx pins each other at the same potential, and leave them unused and floated.

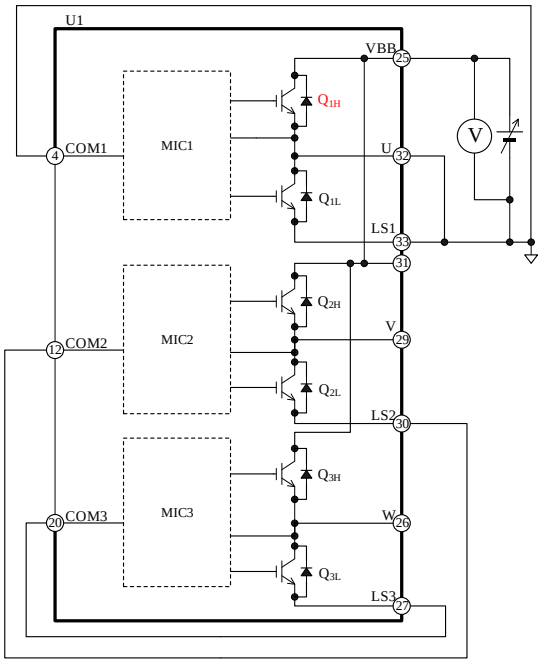


Figure 13-3. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

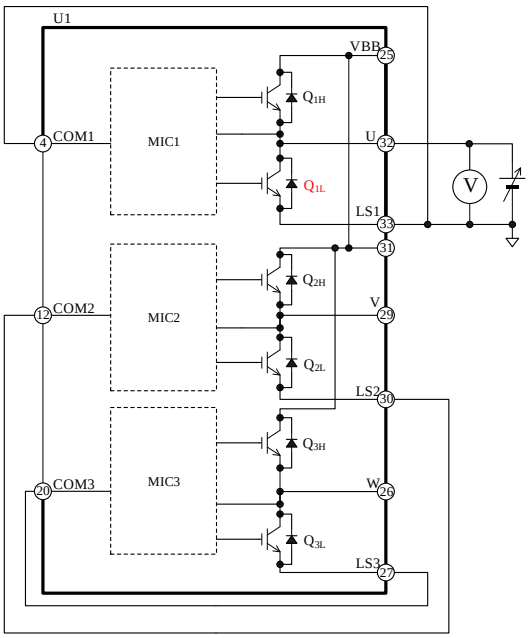


Figure 13-4. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

14. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in a switching transistor, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SCM1200MF series, which is controlled by a 3-phase sine-wave PWM driving strategy. Total power loss in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{SW}. The following subsections contain the mathematical procedures to calculate the power losses in an IGBT and its junction temperature.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0025: SCM1200MF Series Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/scm12xxmf_caltool_en.html

14.1. IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 15.3.1.

As expressed by the curves in Figure 14-1, linear approximations at a range the I_C is actually used are obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (4)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
$\cos\theta$ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and
β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

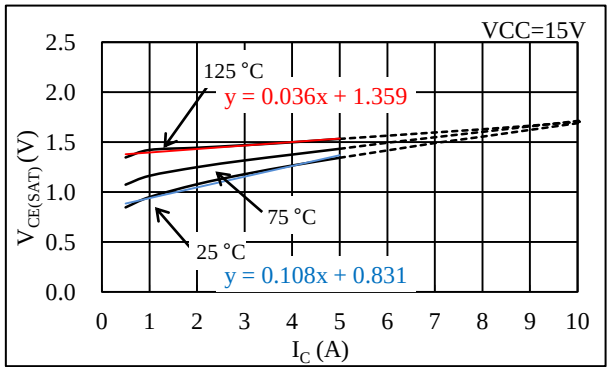


Figure 14-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C Curve

14.2. IGBT Switching Loss, P_{SW}

Switching loss in an IGBT can be calculated by Equation (5), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (5)$$

Where:

f_C is the PWM carrier frequency (Hz),

V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and

α_E is the slope of the switching loss curve (see Section 15.3.2).

14.3. Estimating Junction Temperature of IGBT

The junction temperature of an IGBT, T_j, can be estimated with Equation (6):

$$T_j = R_{(j-c)Q} \times (P_{ON} + P_{SW}) + T_C. \quad (6)$$

Where:

$R_{(j-c)Q}$ is the junction-to-case thermal resistance per IGBT (°C/W), and

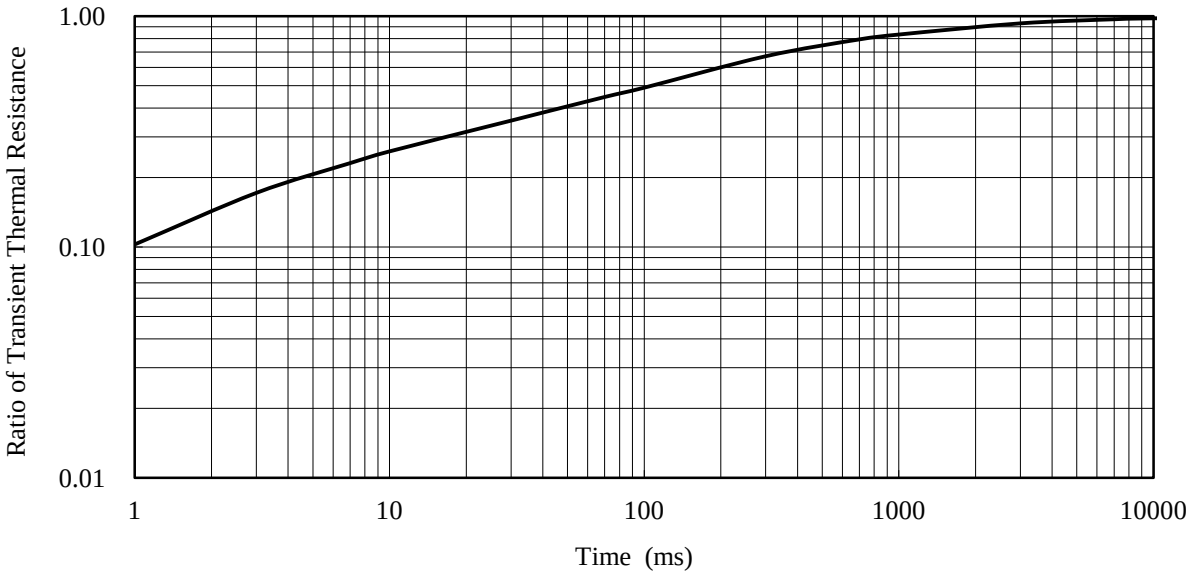
T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

15. Performance Curves

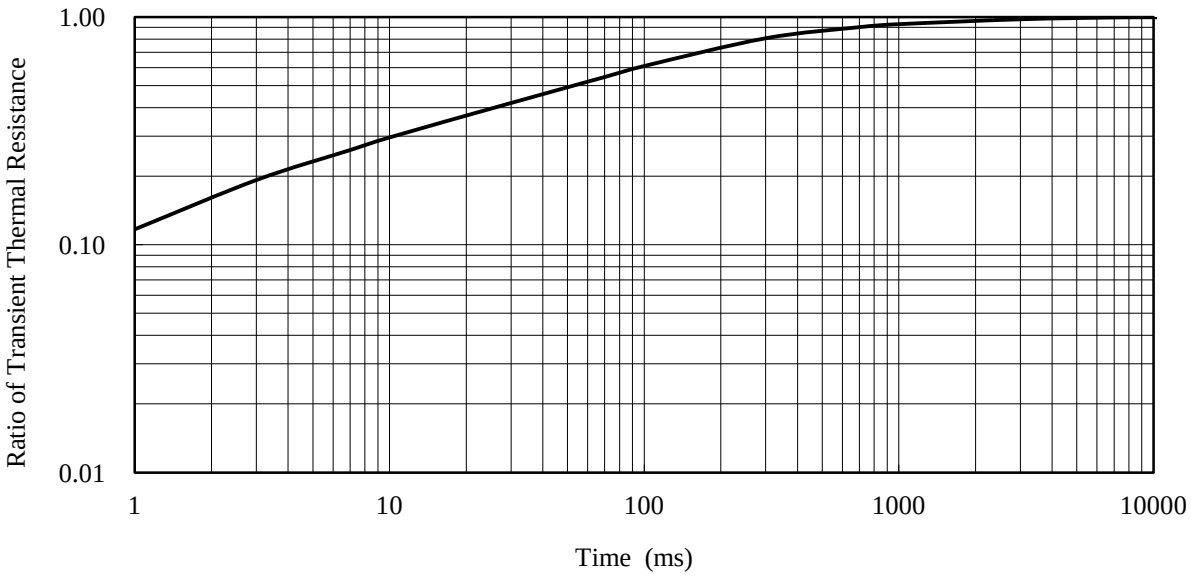
15.1. Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

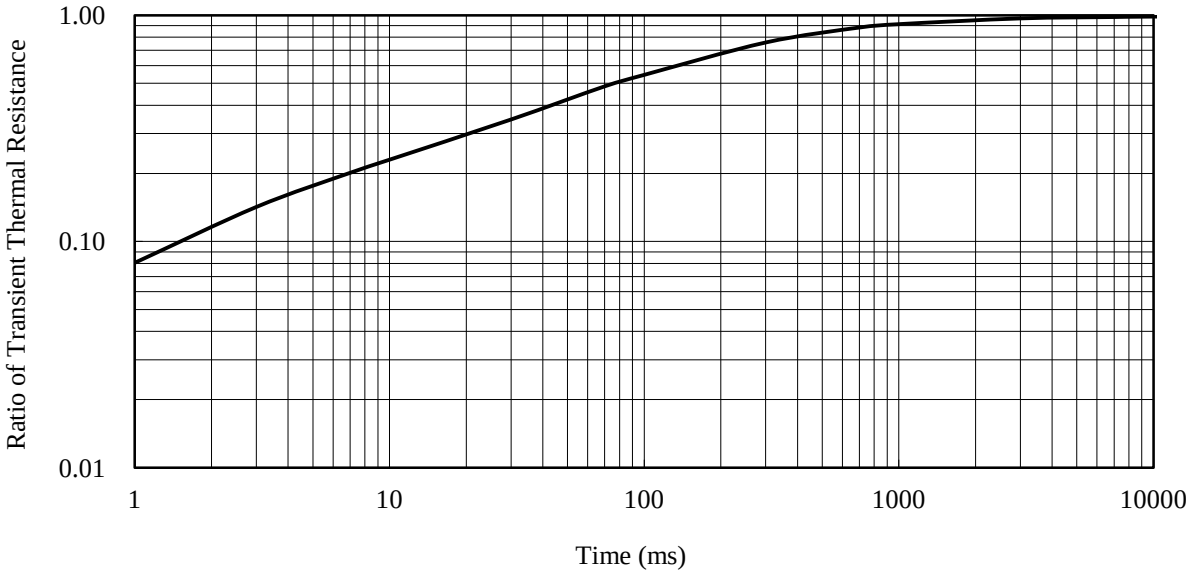
15.1.1. SCM1261MF



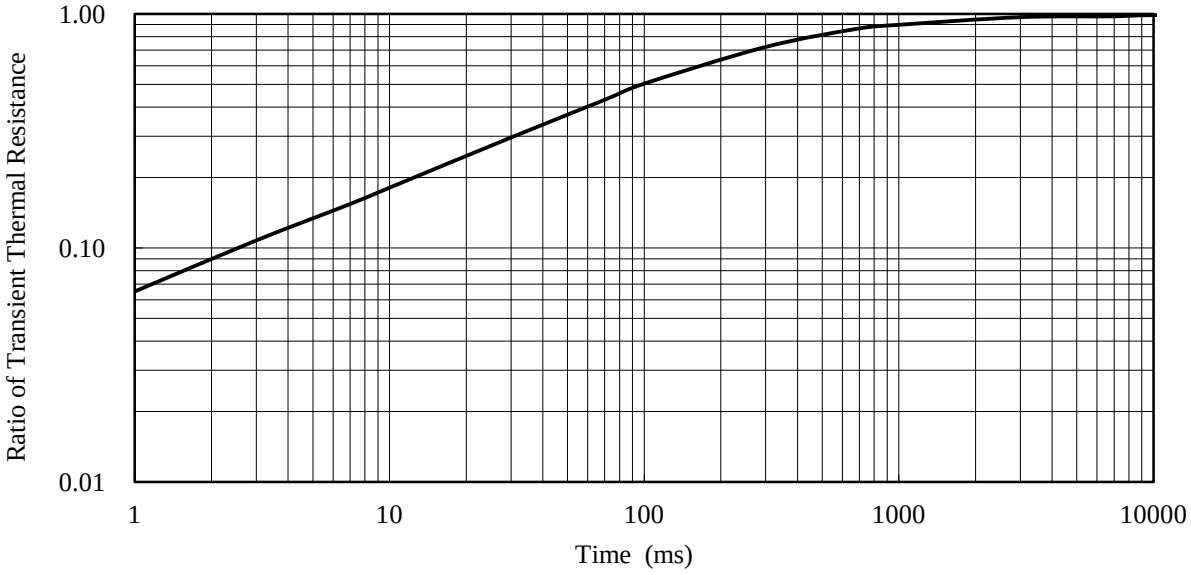
15.1.2. SCM1242MF, SCM1263MF, SCM1243MF



15.1.3. SCM1265MF, SCM1245MF



15.1.4. SCM1246MF, SCM1256MF



15.2. Performance Curves of Control Parts

Figure 15-2 to Figure 15-27 provide performance curves of the control parts integrated in the SCM1200MF series, including variety-dependent characteristics and thermal characteristics. T_j represents the junction temperature of the control parts.

Table 15-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 15-2	Logic Supply Current in 3-phase Operation, I_{CC} vs. T_C
Figure 15-3	Logic Supply Current in 3-phase Operation, I_{CC} vs. VCCx Pin Voltage, V_{CC}
Figure 15-4	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 15-5	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 15-6	Figure 15-1. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B
Figure 15-7	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 15-8	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 15-9	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 15-10	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 15-11	UVLO_VB Filtering Time vs. T_C
Figure 15-12	UVLO_VCC Filtering Time vs. T_C
Figure 15-13	Input Current at High Level (HINx or LINx), I_{IN} vs. T_C
Figure 15-14	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 15-15	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 15-16	High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)
Figure 15-17	High-side Turn-off Propagation Delay vs. T_C (from HINx to HOx)
Figure 15-18	Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)
Figure 15-19	Low-side Turn-off Propagation Delay vs. T_C (from LINx to LOx)
Figure 15-20	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 15-21	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 15-22	Typical Output Pulse Widths, t_{HO}, t_{LO} vs. Input Pulse Widths, t_{HIN}, t_{LIN}
Figure 15-23	FOx Pin Voltage in Normal Operation, V_{FOL} vs. T_C
Figure 15-24	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 15-25	Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C
Figure 15-26	OCP Hold Time, t_P vs. T_C
Figure 15-27	Filtering Time of Simultaneous On-state Prevention vs. T_C

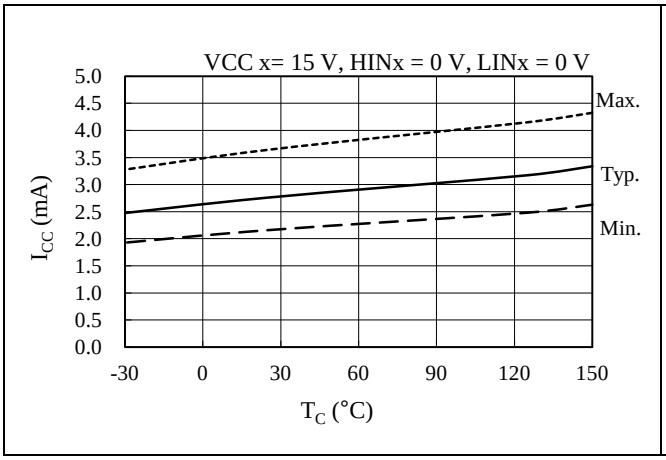


Figure 15-2. Logic Supply Current in 3-phase Operation, I_{CC} vs. T_C

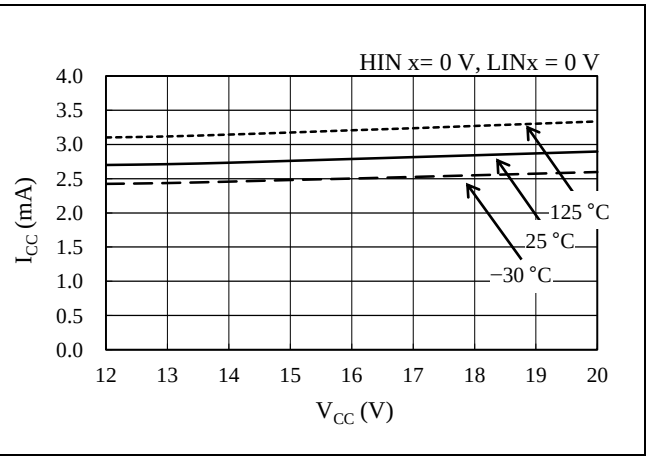


Figure 15-3. Logic Supply Current in 3-phase Operation, I_{CC} vs. VCCx Pin Voltage, V_{CC}

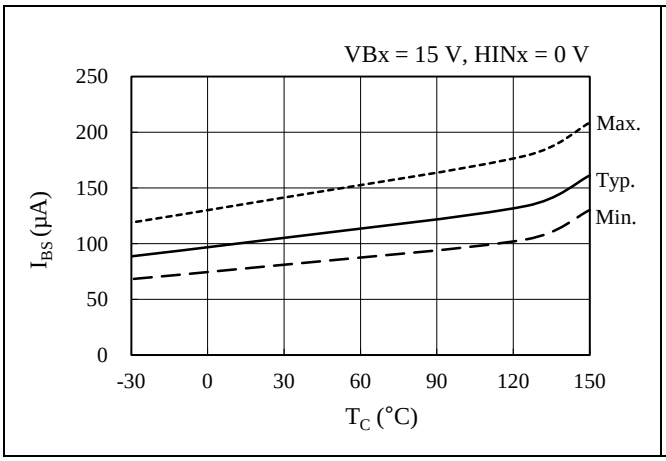


Figure 15-4. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

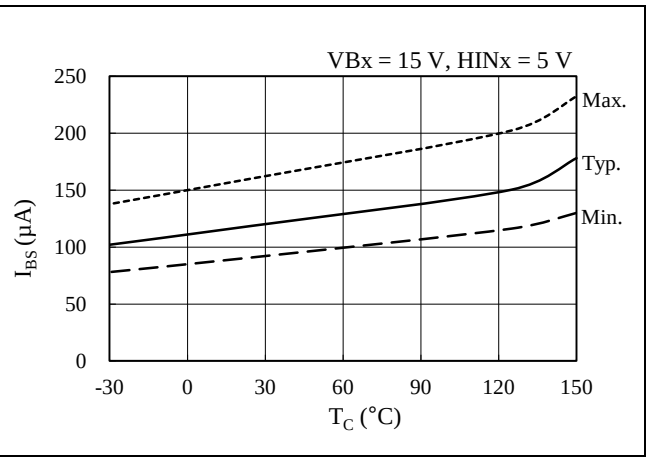


Figure 15-5. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

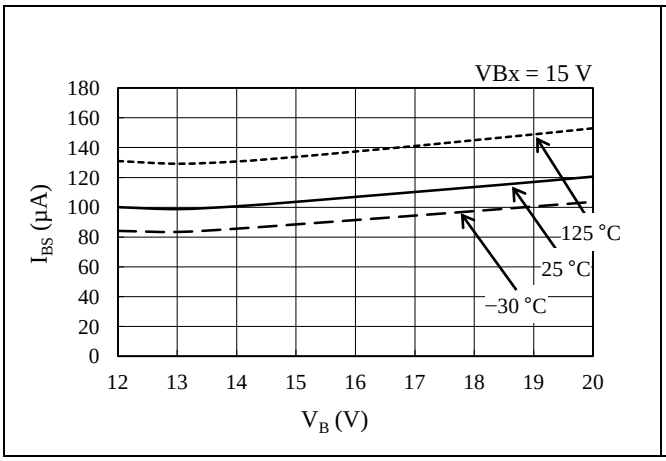


Figure 15-6. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B

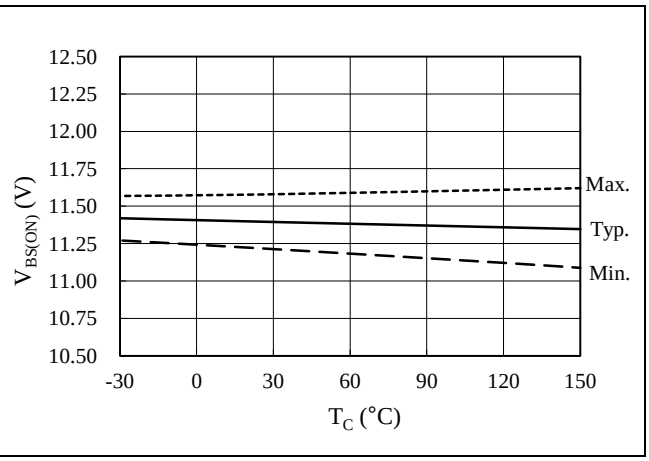


Figure 15-7. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

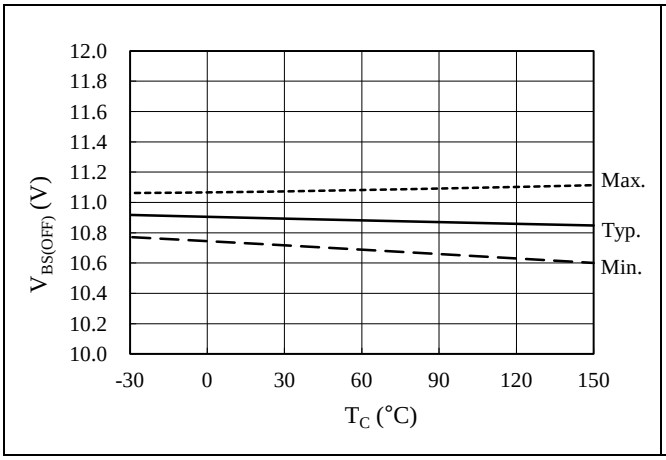


Figure 15-8. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

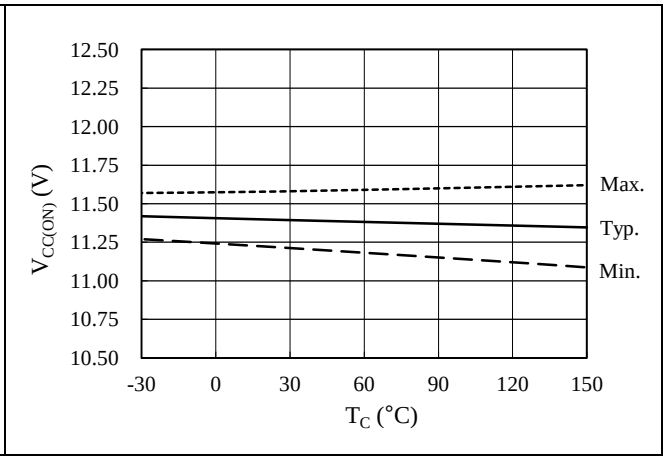


Figure 15-9. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

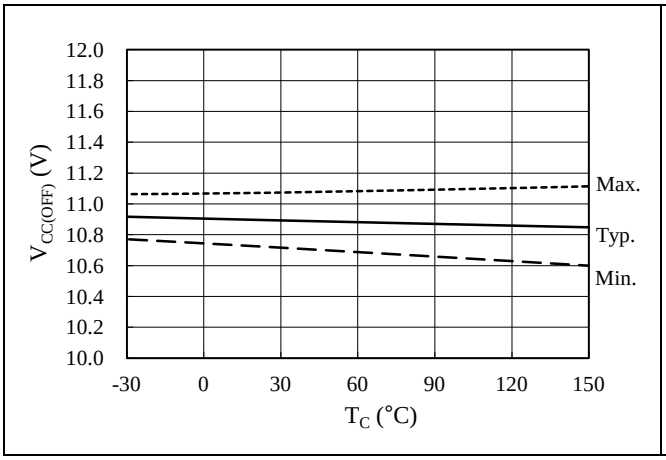


Figure 15-10. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

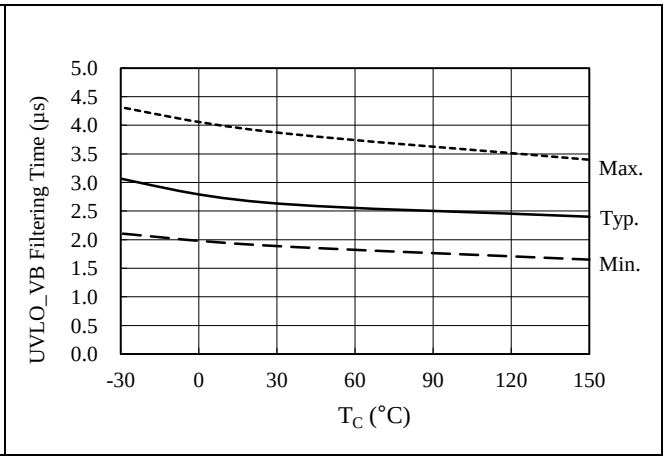


Figure 15-11. UVLO_VB Filtering Time vs. T_C

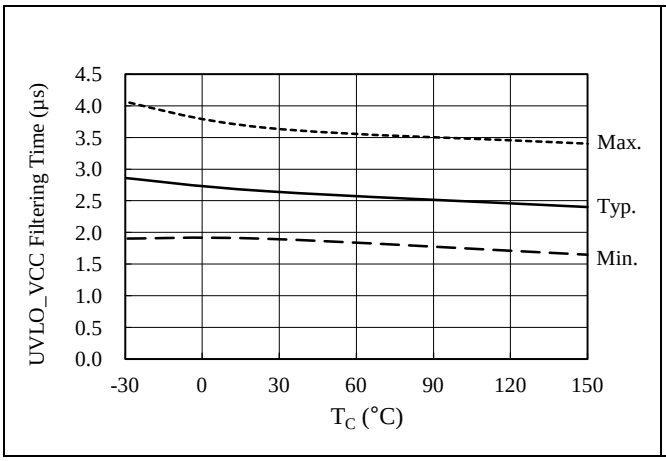


Figure 15-12. UVLO_VCC Filtering Time vs. T_C

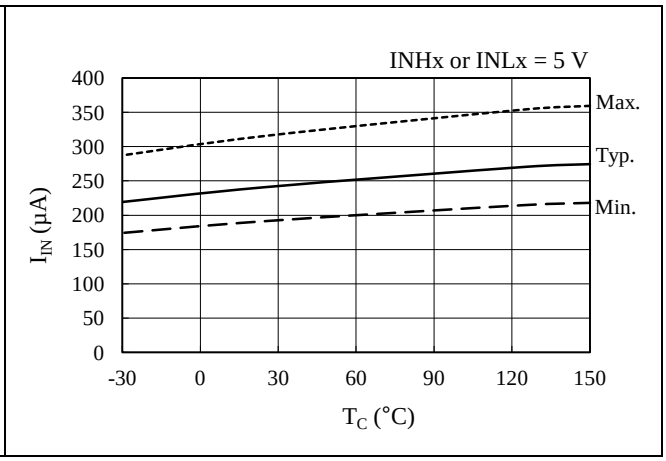


Figure 15-13. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

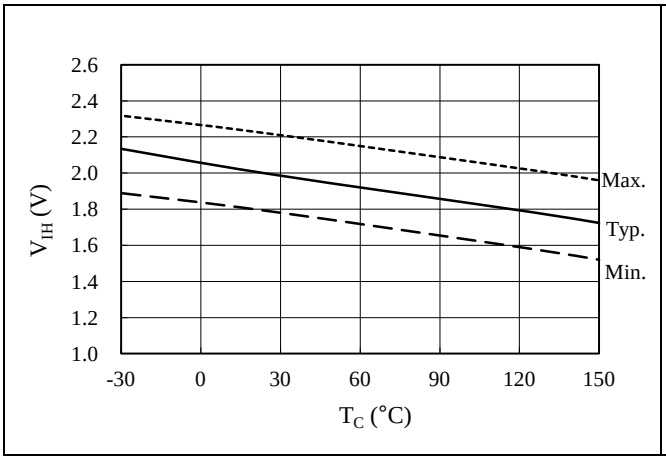


Figure 15-14. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

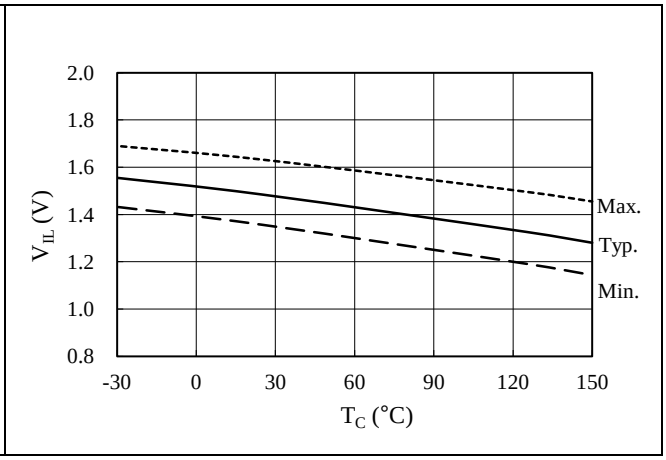


Figure 15-15. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

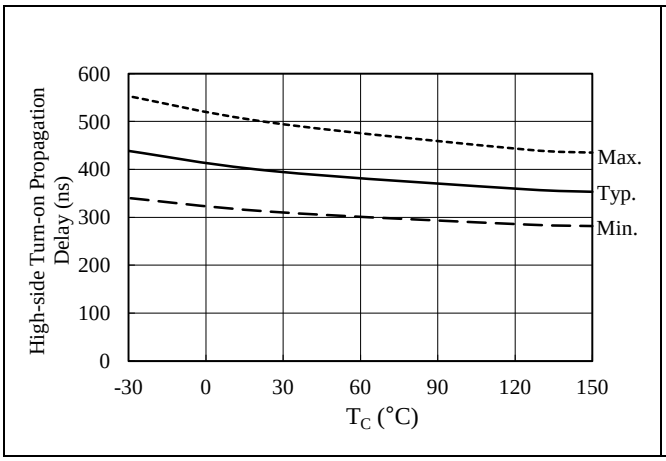


Figure 15-16. High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)

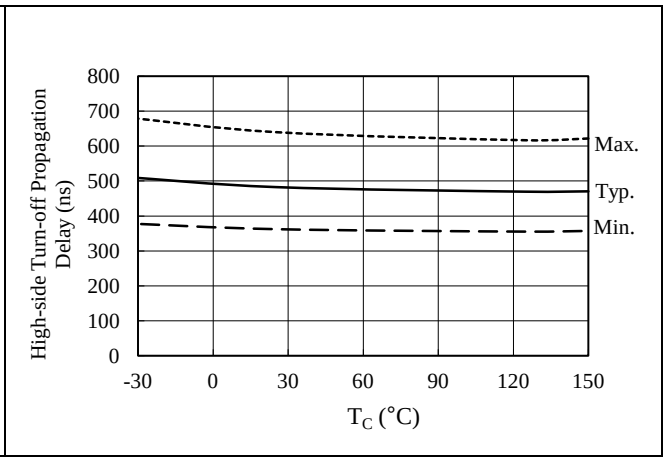


Figure 15-17. High-side Turn-off Propagation Delay vs. T_C (from HINx to HOx)

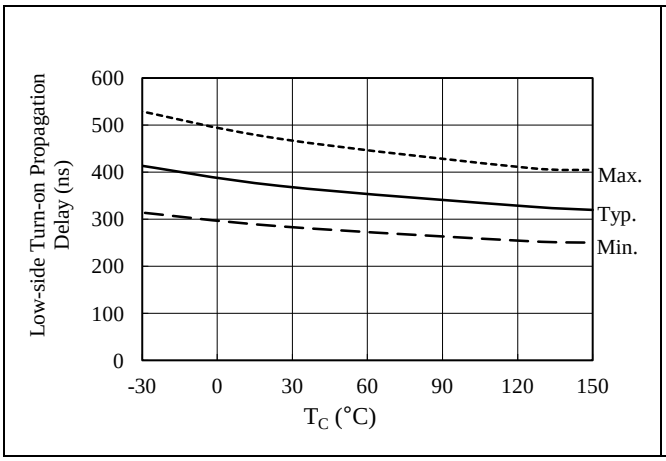


Figure 15-18. Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)

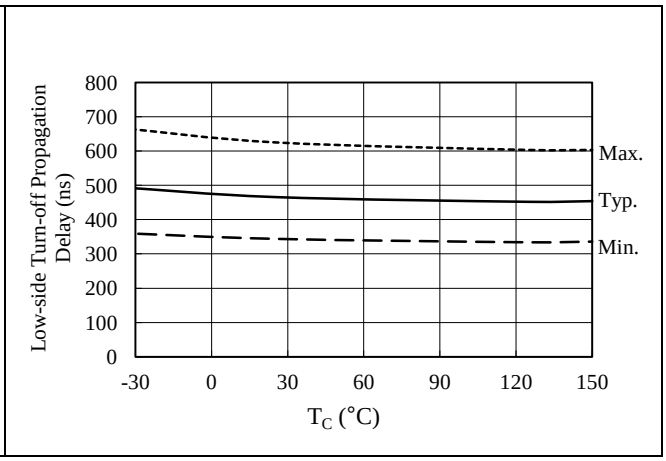


Figure 15-19. Low-side Turn-off Propagation Delay vs. T_C (from LINx to LOx)

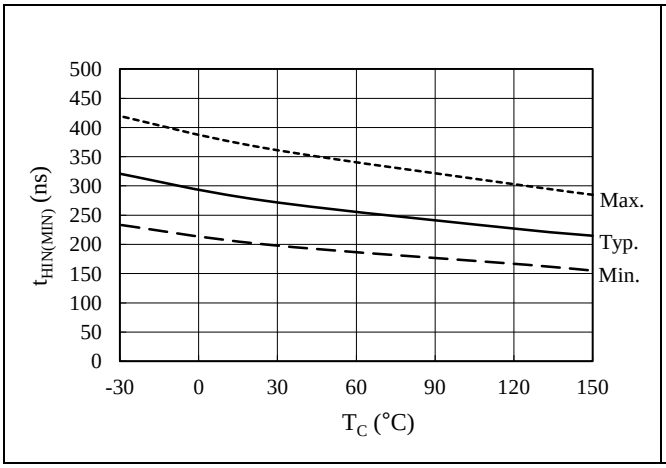


Figure 15-20. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

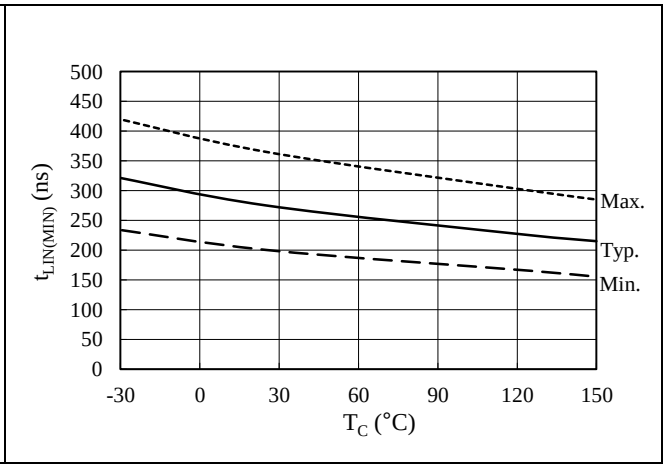


Figure 15-21. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

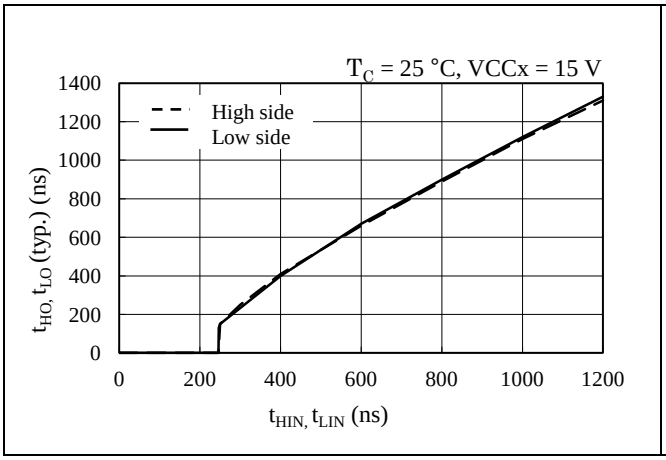


Figure 15-22. Typical Output Pulse Widths, t_{HO}, t_{LO} vs. Input Pulse Widths, t_{HIN}, t_{LIN}

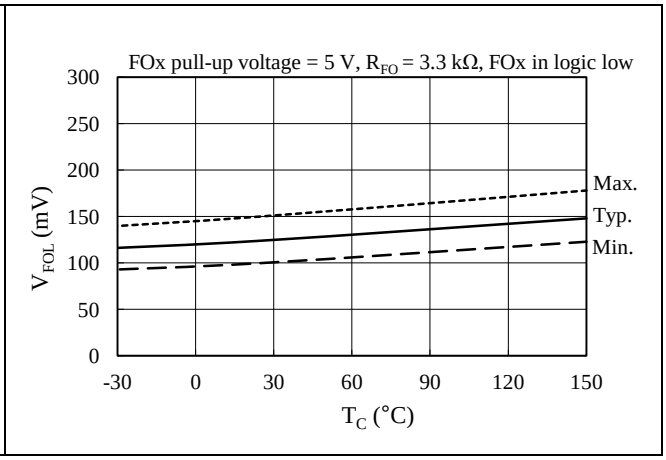


Figure 15-23. FOx Pin Voltage in Normal Operation, V_{FOL} vs. T_C

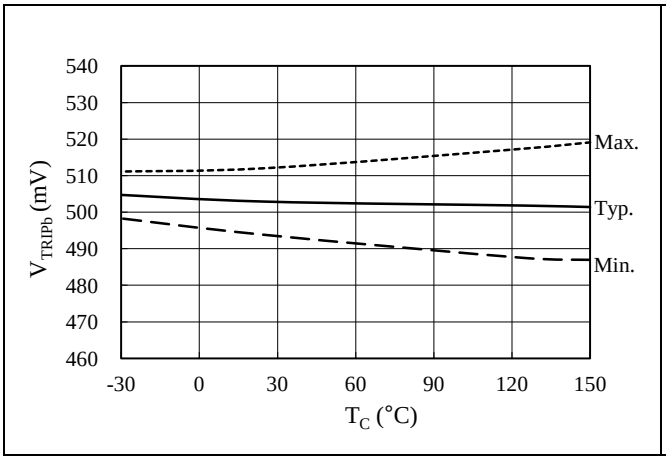


Figure 15-24. OCP Threshold Voltage, V_{TRIP} vs. T_C

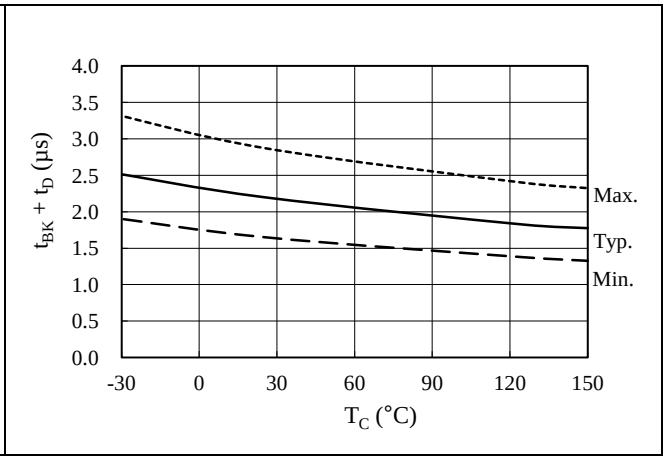


Figure 15-25. Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C

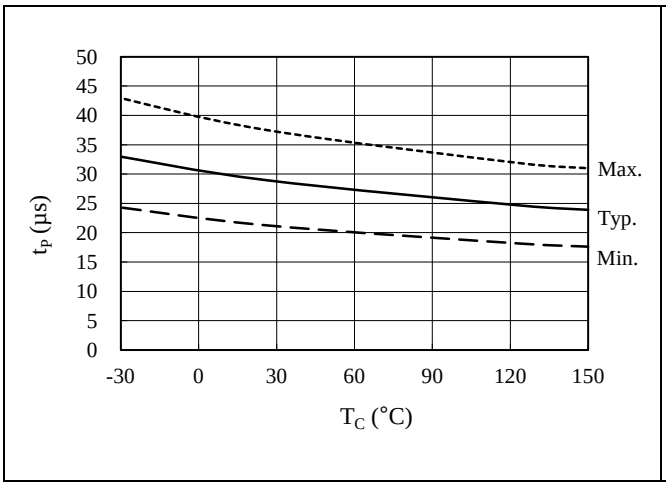


Figure 15-26. OCP Hold Time, t_P vs. T_C

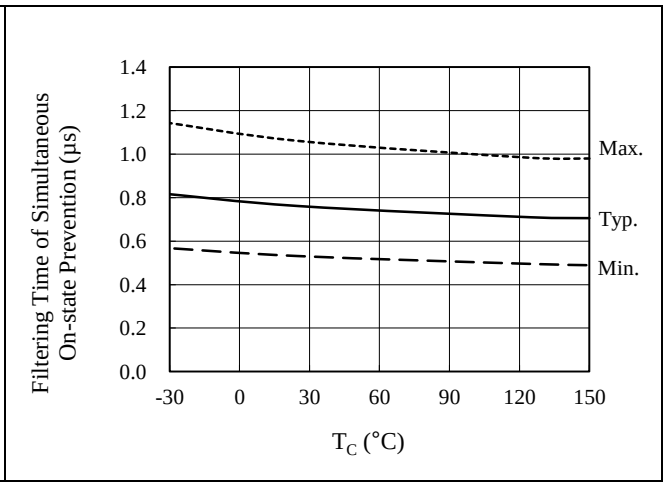


Figure 15-27. Filtering Time of Simultaneous On-state Prevention vs. T_C

15.3. Performance Curves of Output Parts

15.3.1. Output Transistor Performance Curves

15.3.1.1. SCM1261M

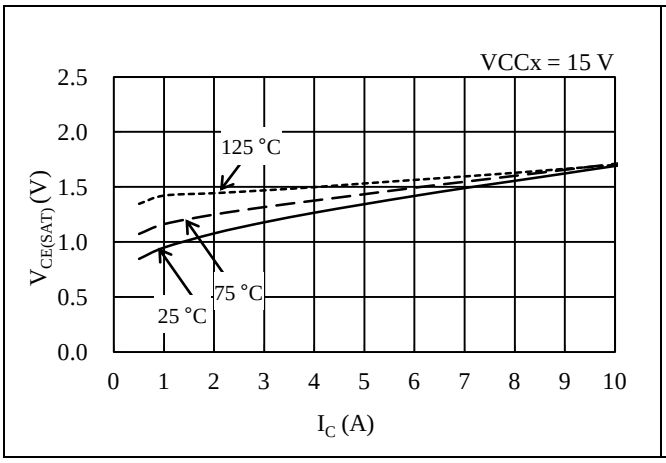


Figure 15-28. IGBT $V_{CE(SAT)}$ vs. I_C

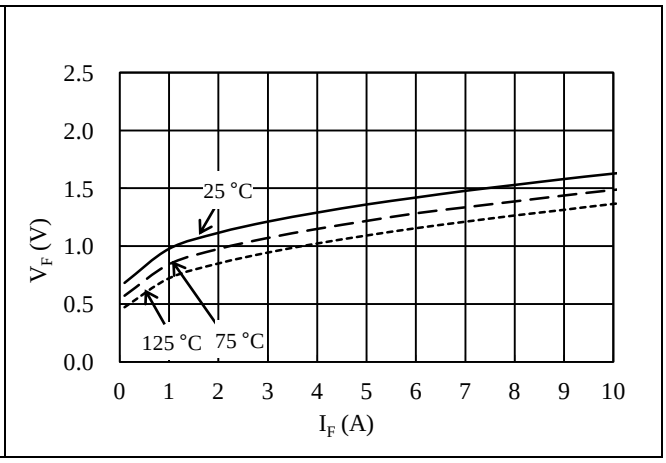


Figure 15-29. Freewheeling Diode V_F vs. I_F

15.3.1.2. SCM1242MF, SCM1263MF, SCM1243MF

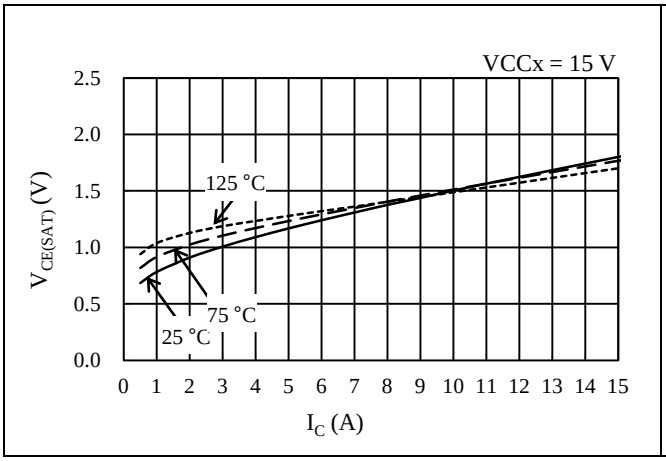


Figure 15-30. IGBT $V_{CE(SAT)}$ vs. I_C

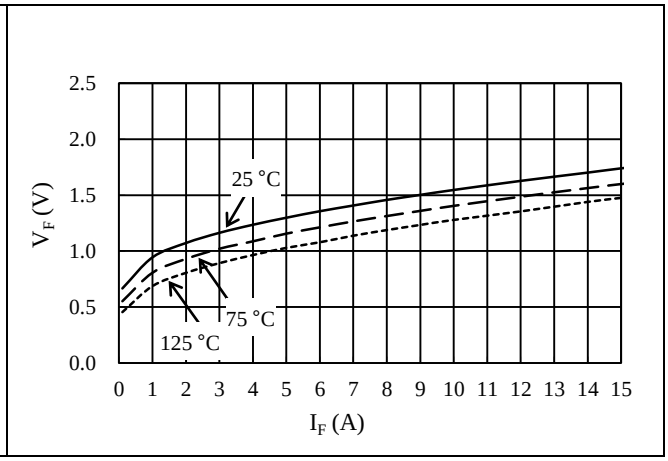


Figure 15-31. Freewheeling Diode V_F vs. I_F

15.3.1.3. SCM1265MF, SCM1245MF

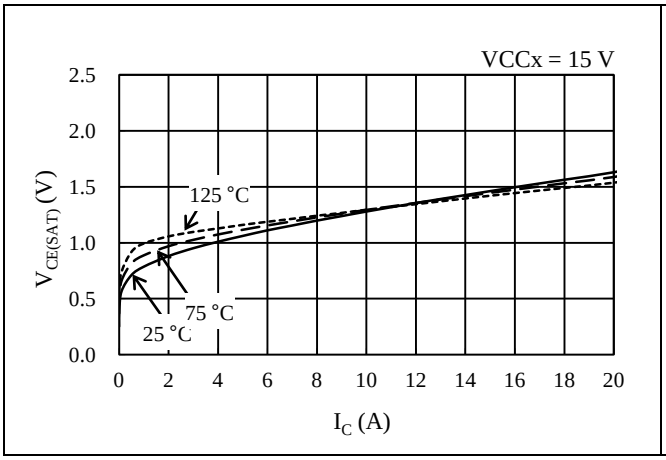


Figure 15-32. IGBT $V_{CE(SAT)}$ vs. I_C

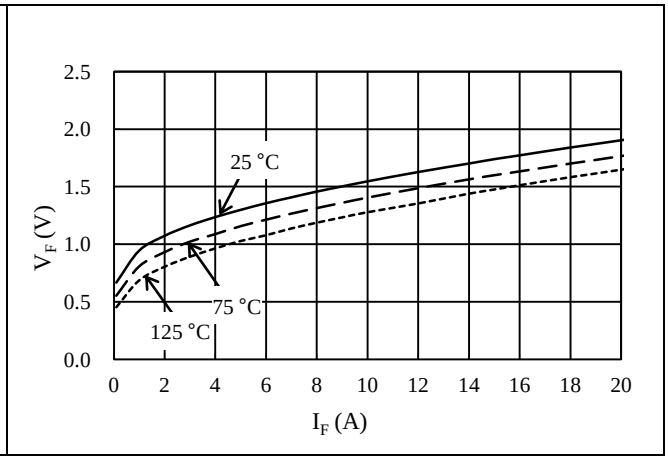


Figure 15-33. Freewheeling Diode V_F vs. I_F

15.3.1.4. SCM1256MF, SCM1246MF

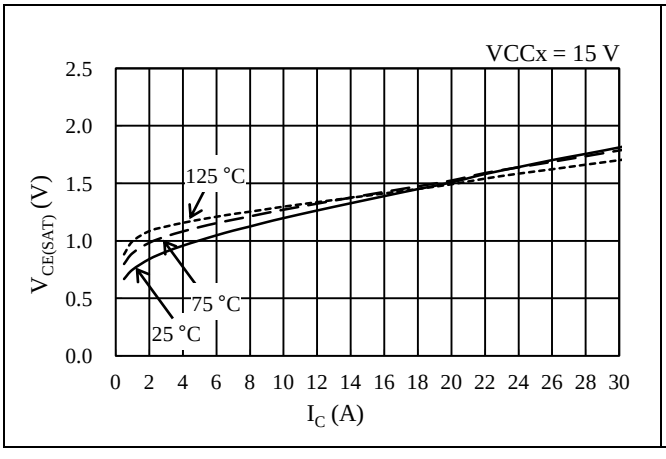


Figure 15-34. IGBT $V_{CE(SAT)}$ vs. I_C

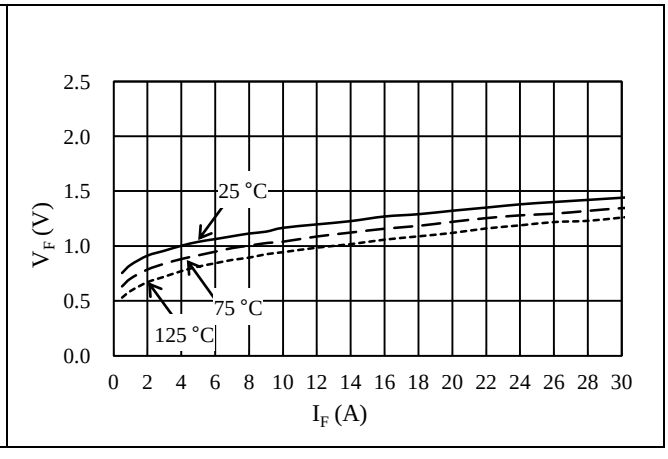


Figure 15-35. Freewheeling Diode V_F vs. I_F

15.3.2. Switching Losses

Conditions: VBB = 300 V, half-bridge circuit with inductive load.

15.3.2.1. SCM1261MF

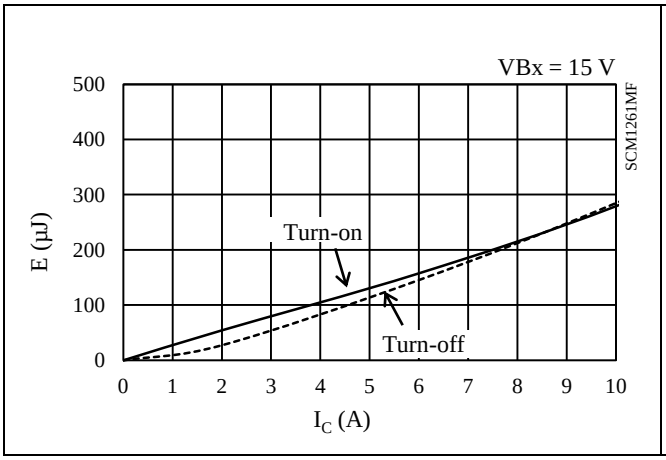


Figure 15-36. High-side Switching Loss (T_j = 25 °C)

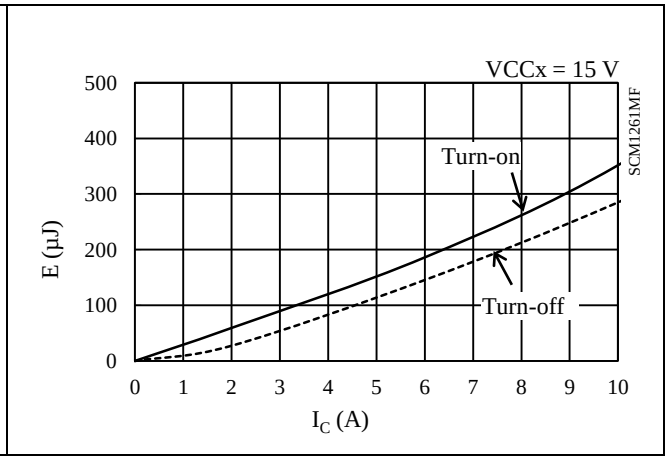


Figure 15-37. Low-side Switching Loss (T_j = 25 °C)

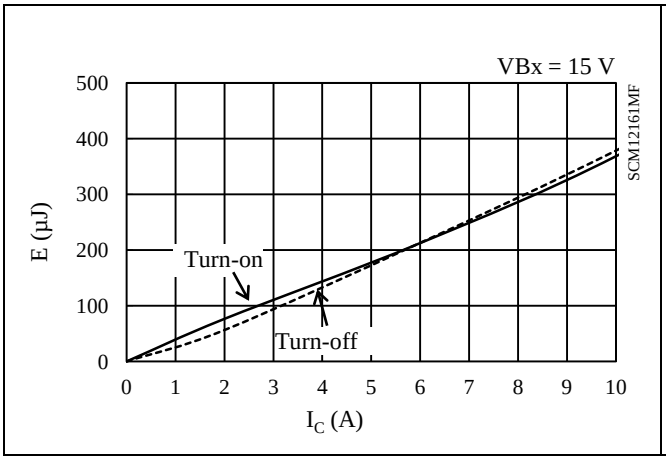


Figure 15-38. High-side Switching Loss (T_j = 125 °C)

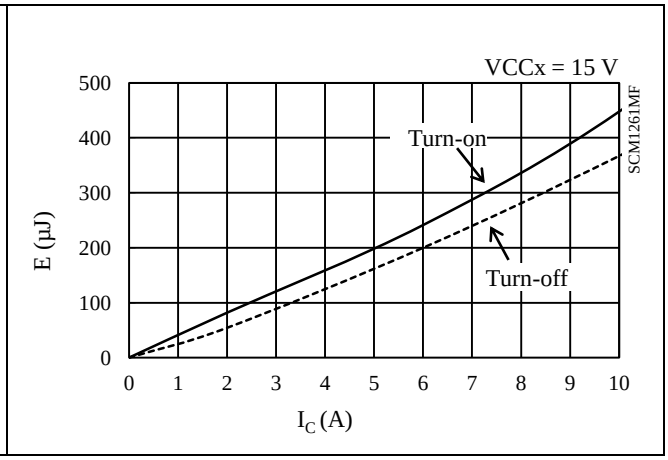


Figure 15-39. Low-side Switching Loss (T_j = 125 °C)

15.3.2.2. SCM1242MF

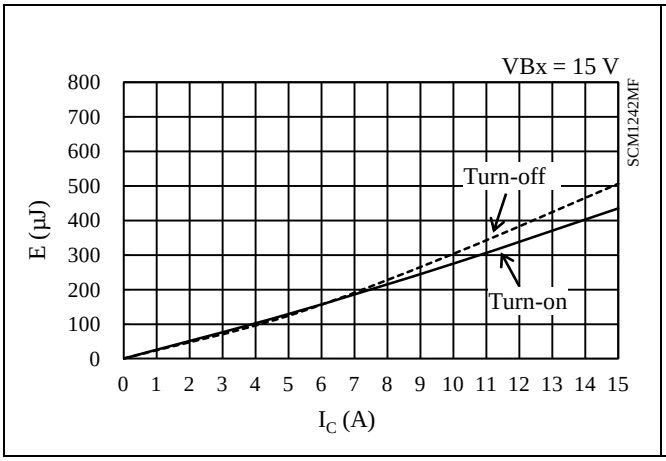


Figure 15-40 High-side Switching Loss (T_j = 25 °C)

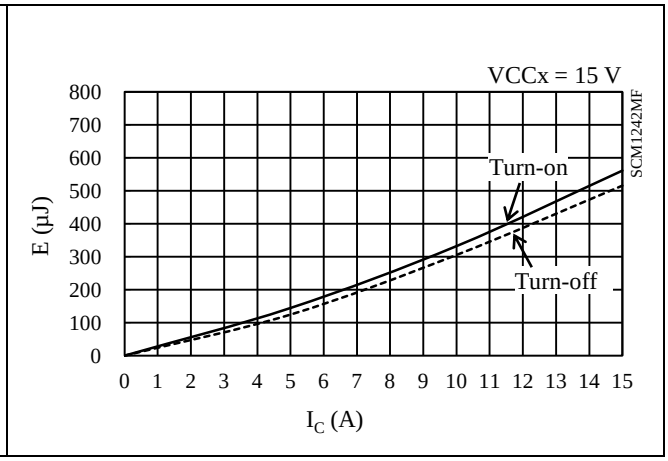


Figure 15-41. Low-side Switching Loss (T_j = 25 °C)

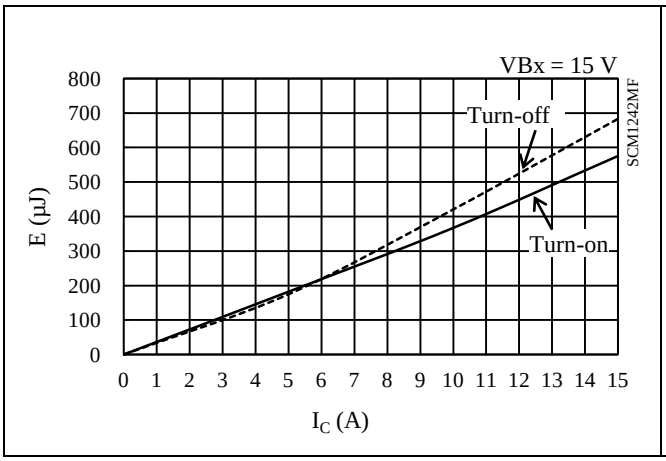


Figure 15-42. High-side Switching Loss (T_j = 125 °C)

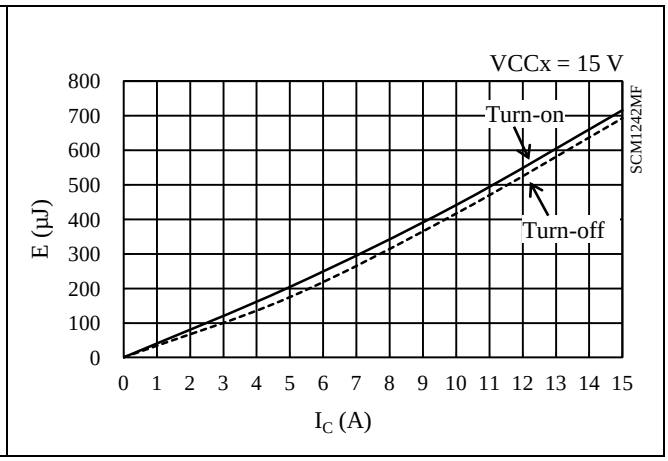


Figure 15-43. Low-side Switching Loss (T_j = 125 °C)

15.3.2.3. SCM1263MF

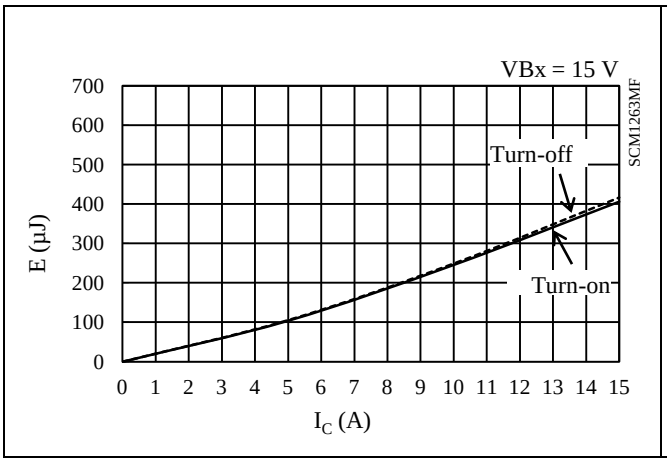


Figure 15-44 High-side Switching Loss (T_j = 25 °C)

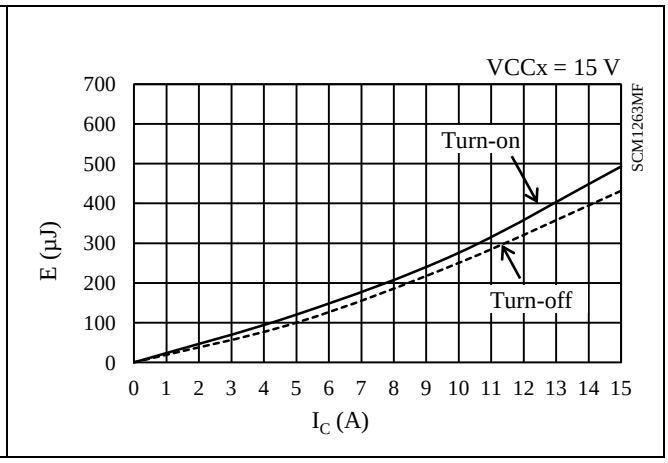


Figure 15-45. Low-side Switching Loss (T_j = 25 °C)

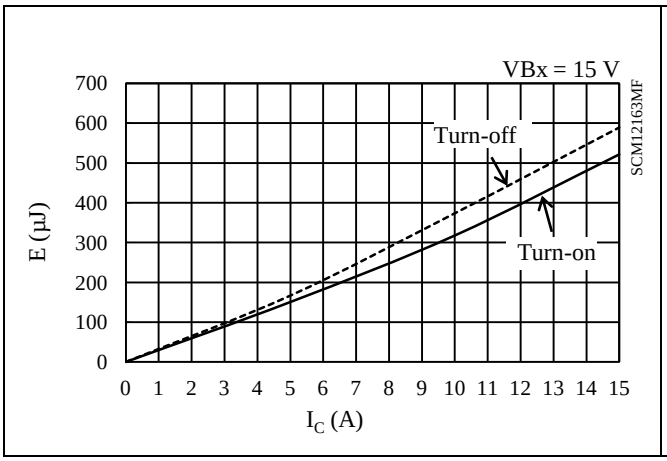


Figure 15-46. High-side Switching Loss (T_j = 125 °C)

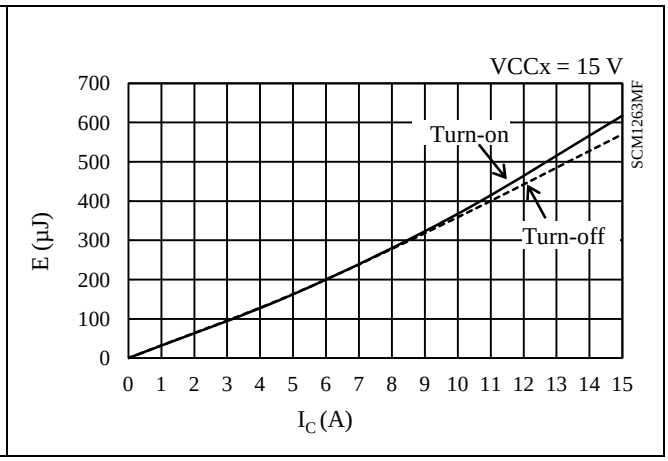


Figure 15-47. Low-side Switching Loss (T_j = 125 °C)

15.3.2.4. SCM1243MF

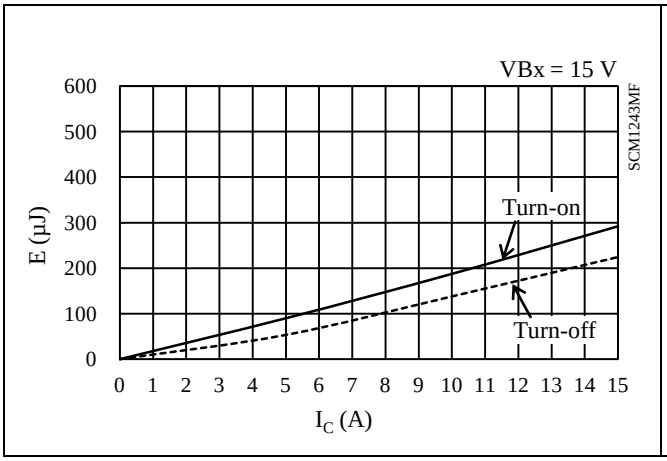


Figure 15-48 High-side Switching Loss (T_j = 25 °C)

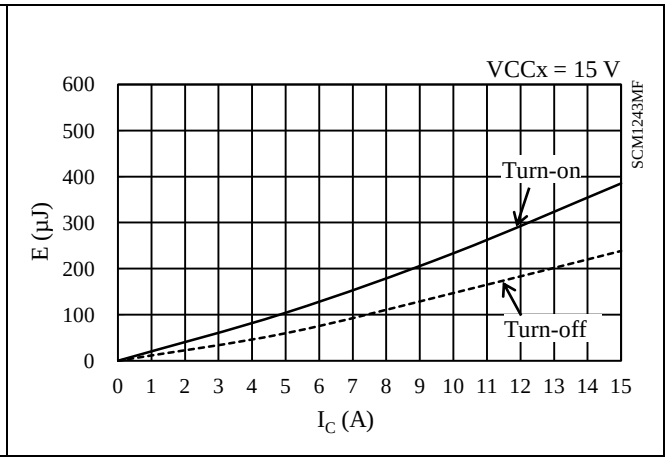


Figure 15-49. Low-side Switching Loss (T_j = 25 °C)

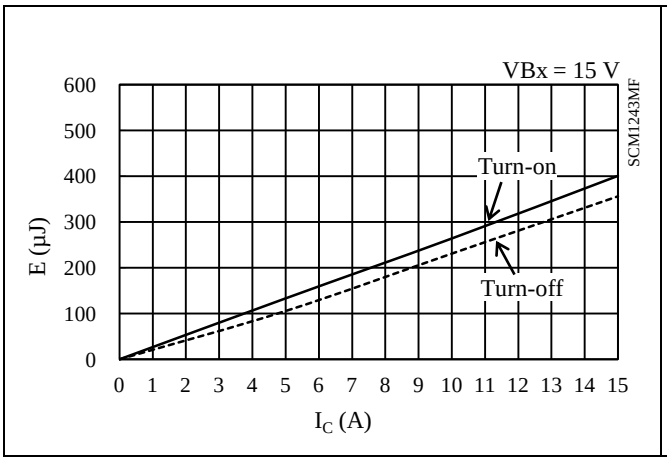


Figure 15-50. High-side Switching Loss (T_j = 125 °C)

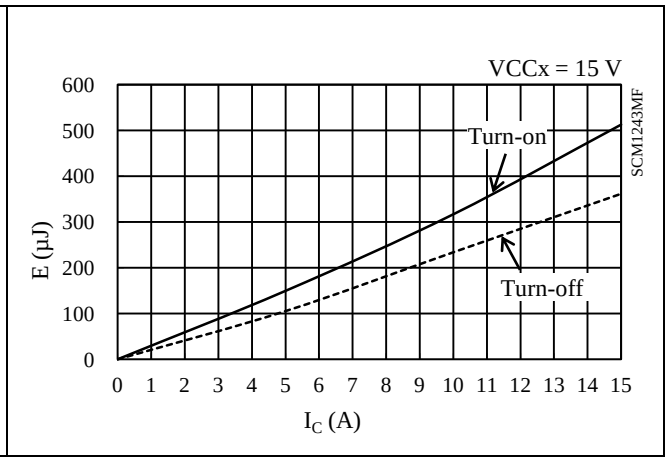


Figure 15-51. Low-side Switching Loss (T_j = 125 °C)

15.3.2.5. SCM1265MF

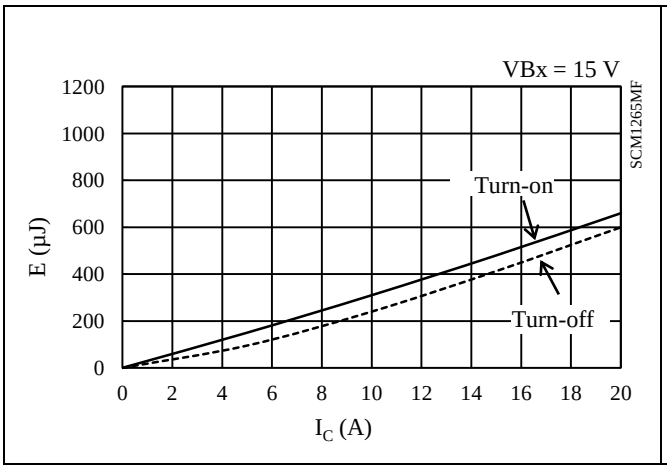


Figure 15-52 High-side Switching Loss (T_j = 25 °C)

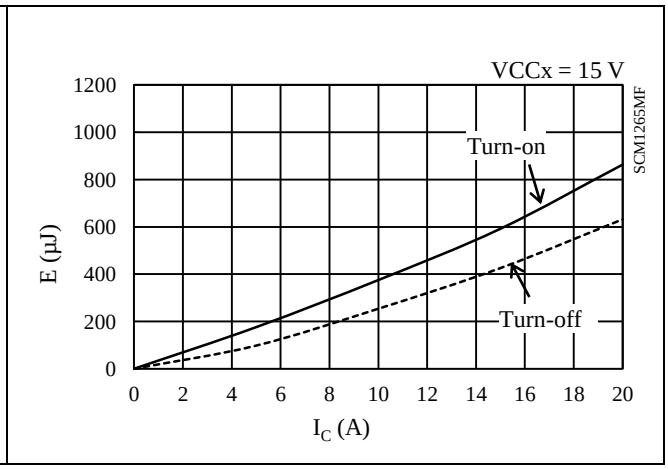


Figure 15-53. Low-side Switching Loss (T_j = 25 °C)

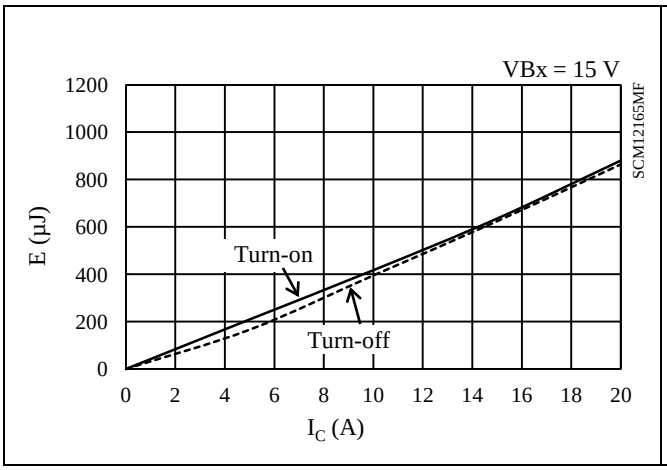


Figure 15-54. High-side Switching Loss (T_j = 125 °C)

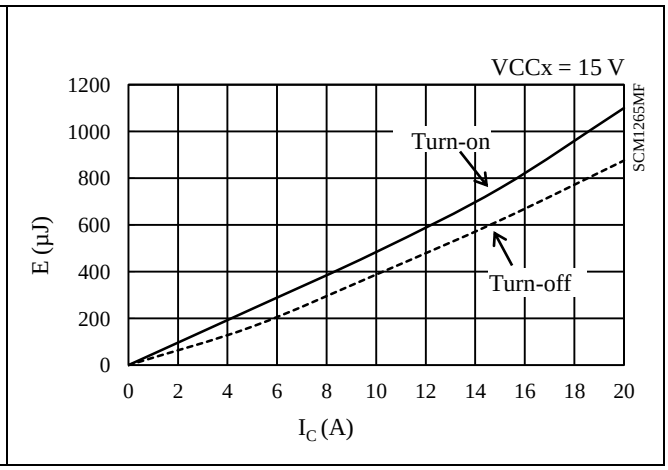


Figure 15-55. Low-side Switching Loss (T_j = 125 °C)

15.3.2.6. SCM1245MF

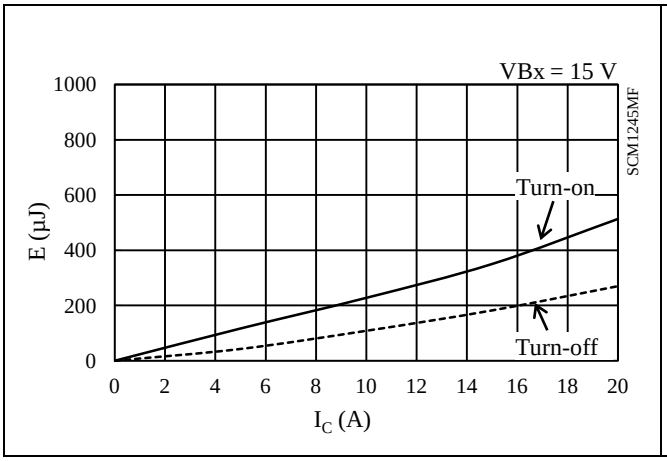


Figure 15-56. High-side Switching Loss (T_j = 25 °C)

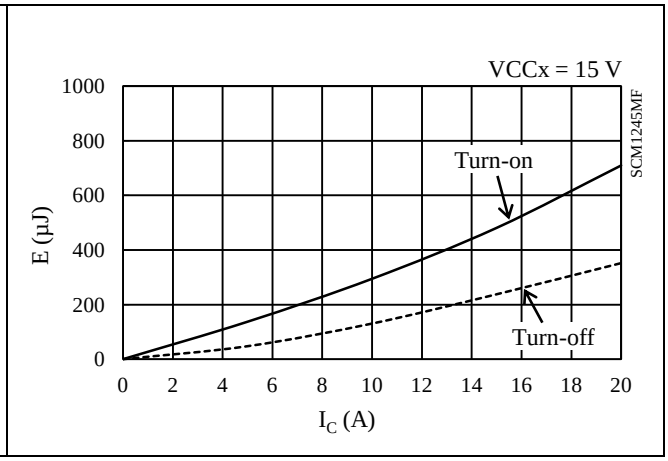


Figure 15-57. Low-side Switching Loss (T_j = 25 °C)

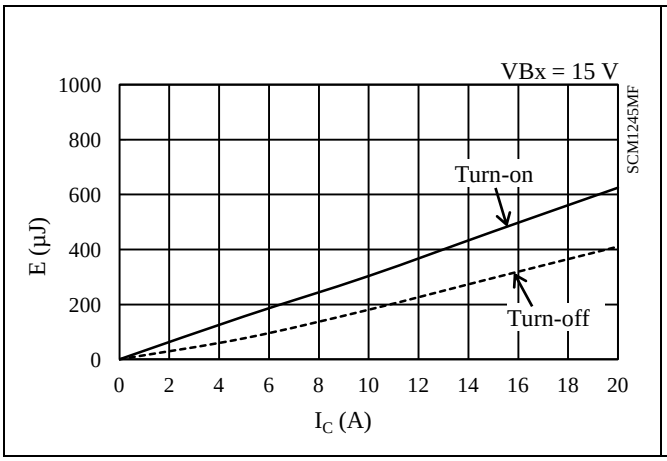


Figure 15-58. High-side Switching Loss (T_j = 125 °C)

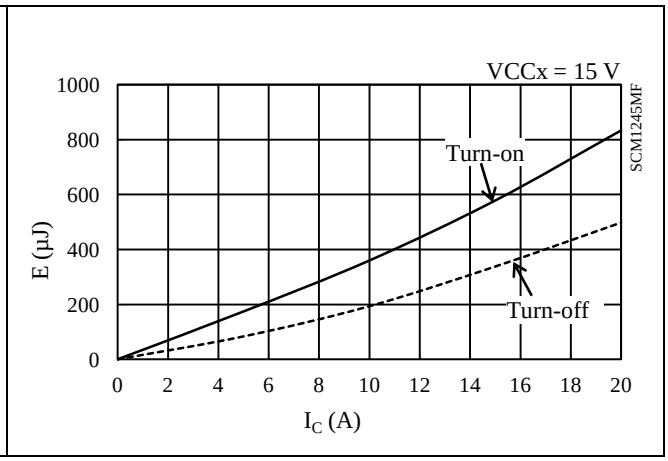


Figure 15-59. Low-side Switching Loss (T_j = 125 °C)

15.3.2.7. SCM1256MF

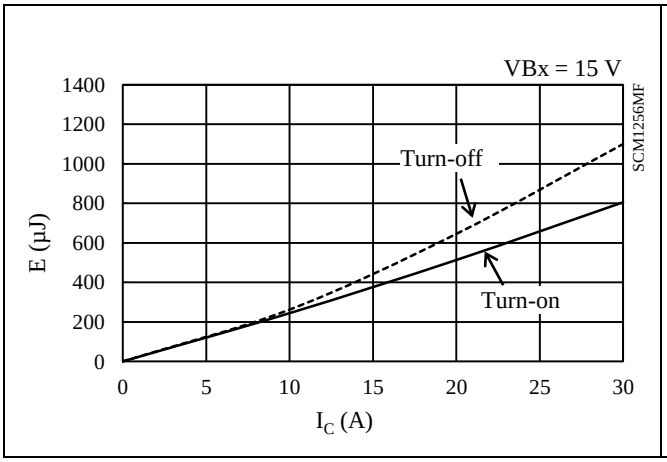


Figure 15-60. High-side Switching Loss (T_j = 25 °C)

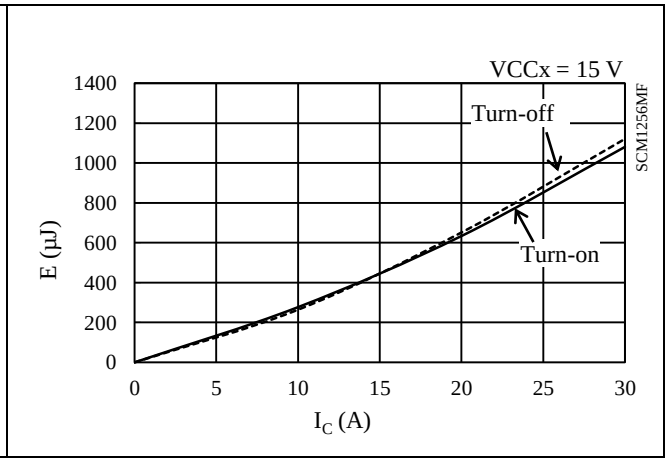


Figure 15-61. Low-side Switching Loss (T_j = 25 °C)

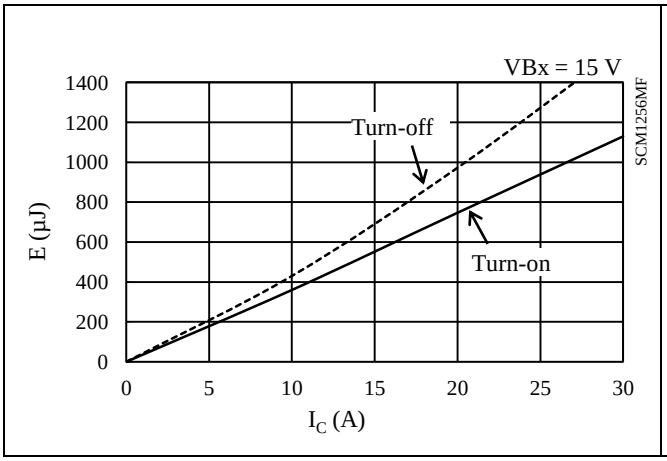


Figure 15-62. High-side Switching Loss (T_j = 125 °C)

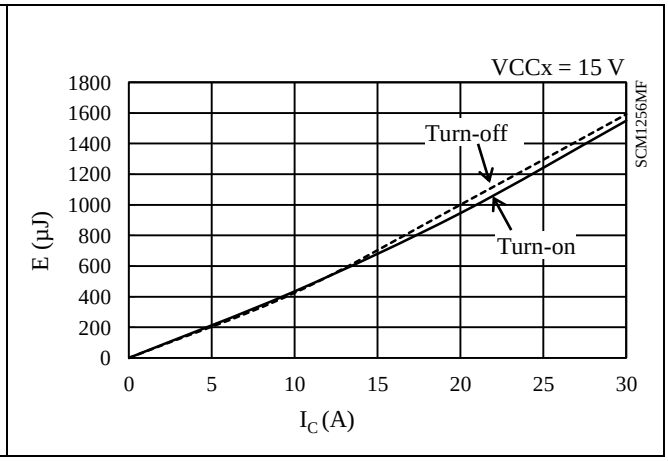


Figure 15-63. Low-side Switching Loss (T_j = 125 °C)

15.3.2.8. SCM1246MF

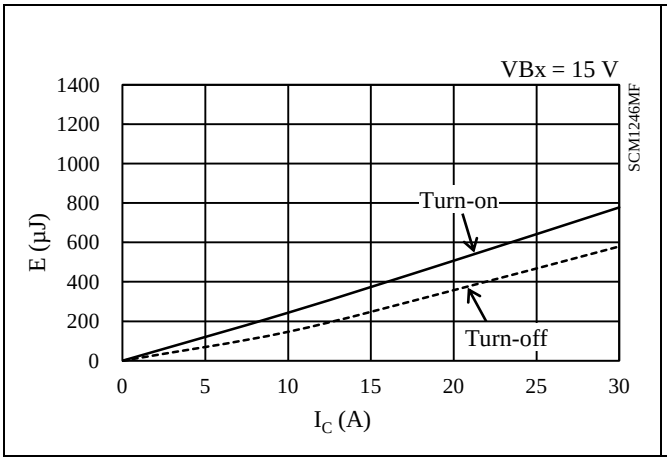


Figure 15-64. High-side Switching Loss (T_j = 25 °C)

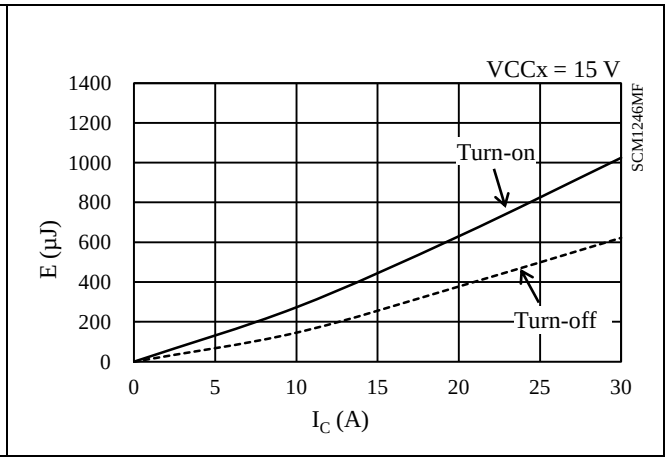


Figure 15-65. Low-side Switching Loss (T_j = 25 °C)

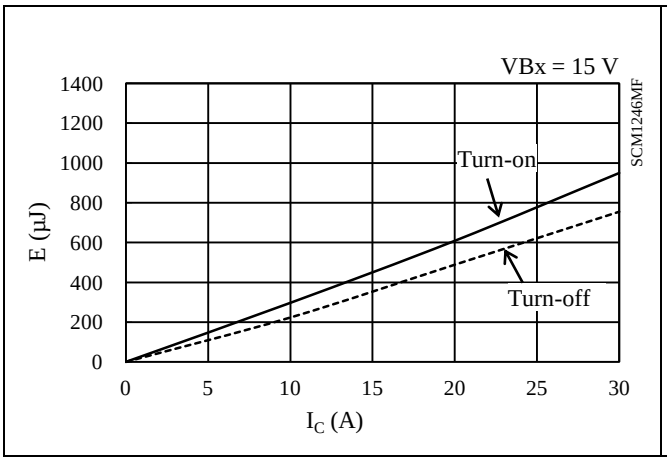


Figure 15-66. High-side Switching Loss (T_j = 125 °C)

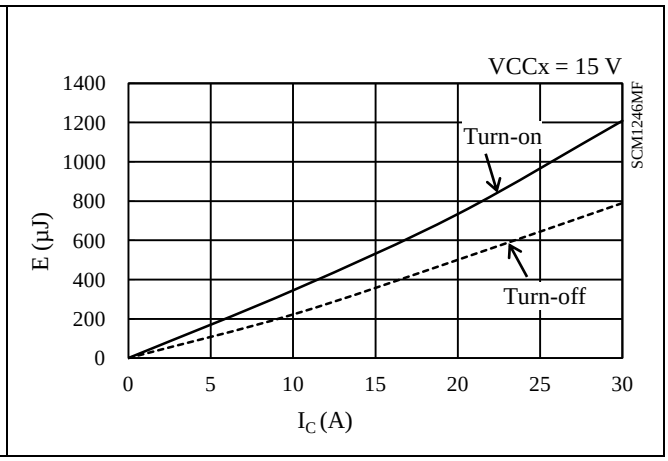


Figure 15-67. Low-side Switching Loss (T_j = 125 °C)

15.4. Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $V_{CE(SAT)}$ and typical switching losses.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_j = 150 °C.

15.4.1. SCM1261MF

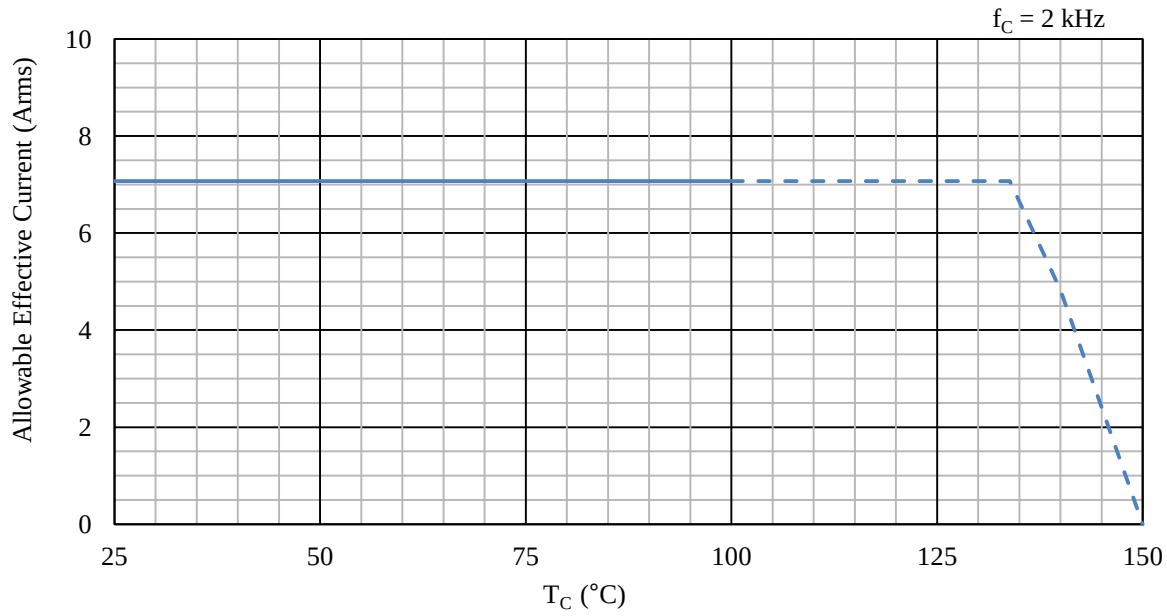


Figure 15-68. Allowable Effective Current (f_C = 2 kHz): 10 A Device

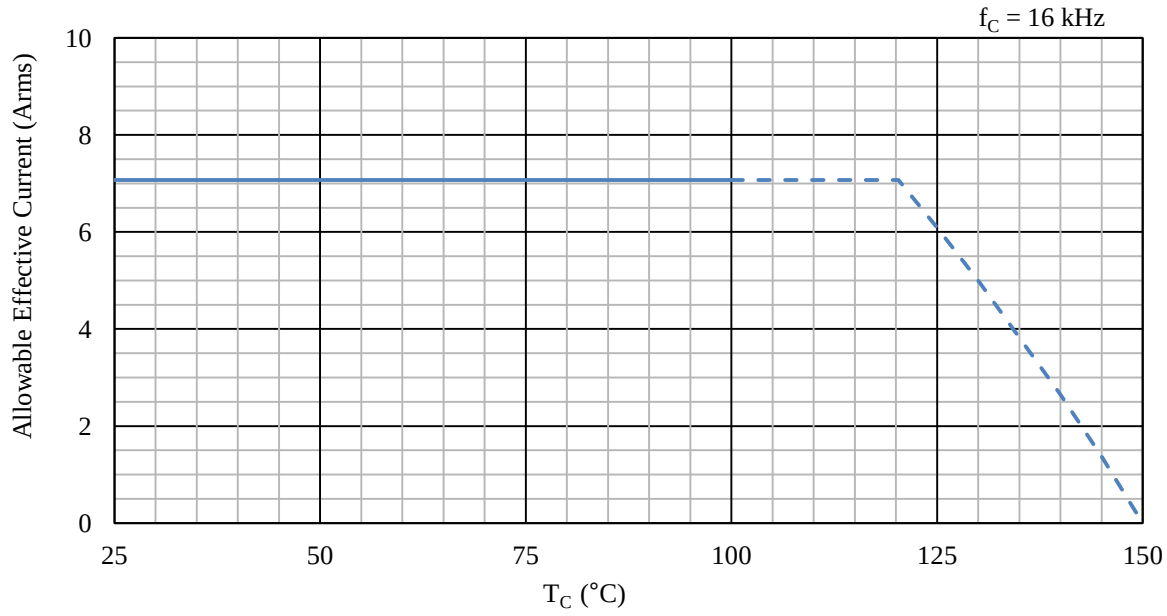


Figure 15-69. Allowable Effective Current (f_C = 16 kHz): 10 A Device

15.4.2. SCM1242MF, SCM1263MF, SCM1243MF

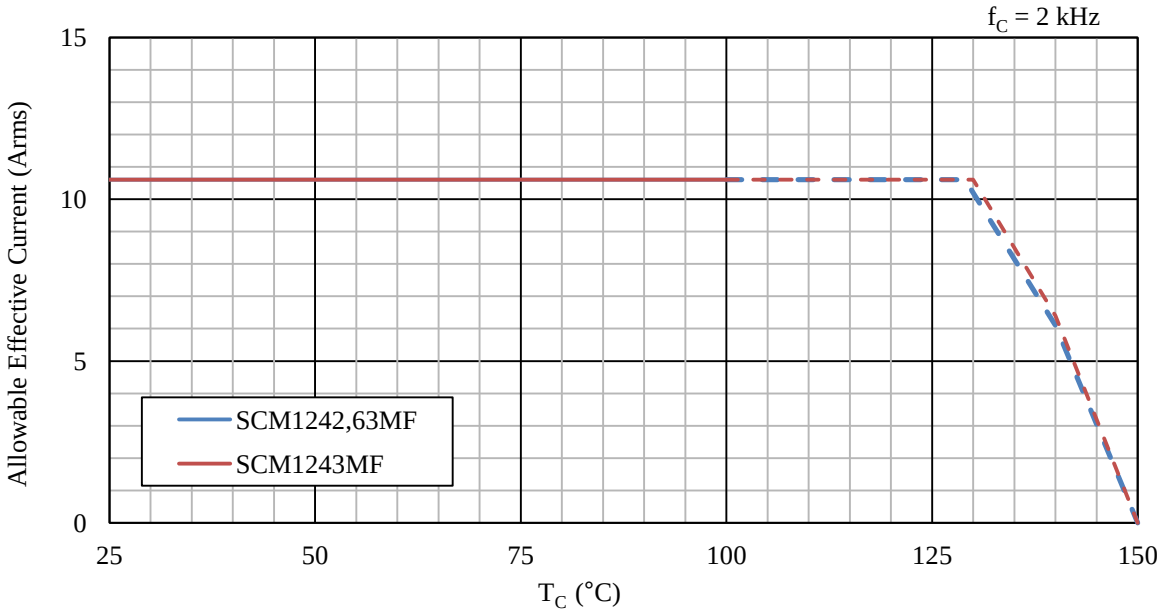


Figure 15-70. Allowable Effective Current (f_C = 2 kHz): 15 A Devices

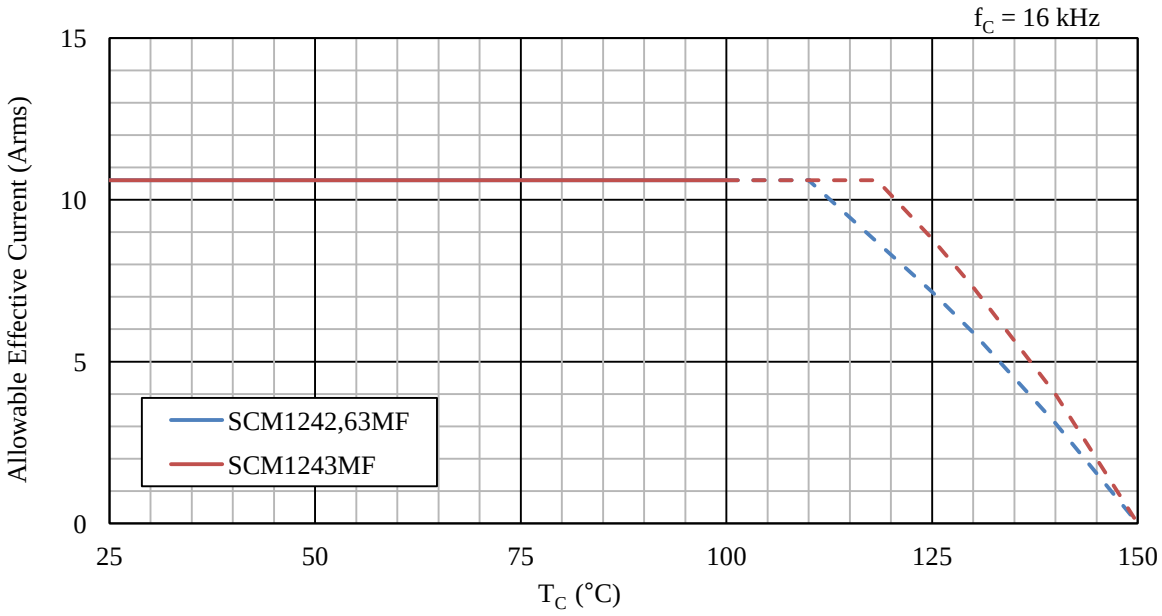


Figure 15-71. Allowable Effective Current (f_C = 16 kHz): 15 A Devices

15.4.3. SCM1265MF, SCM1245MF

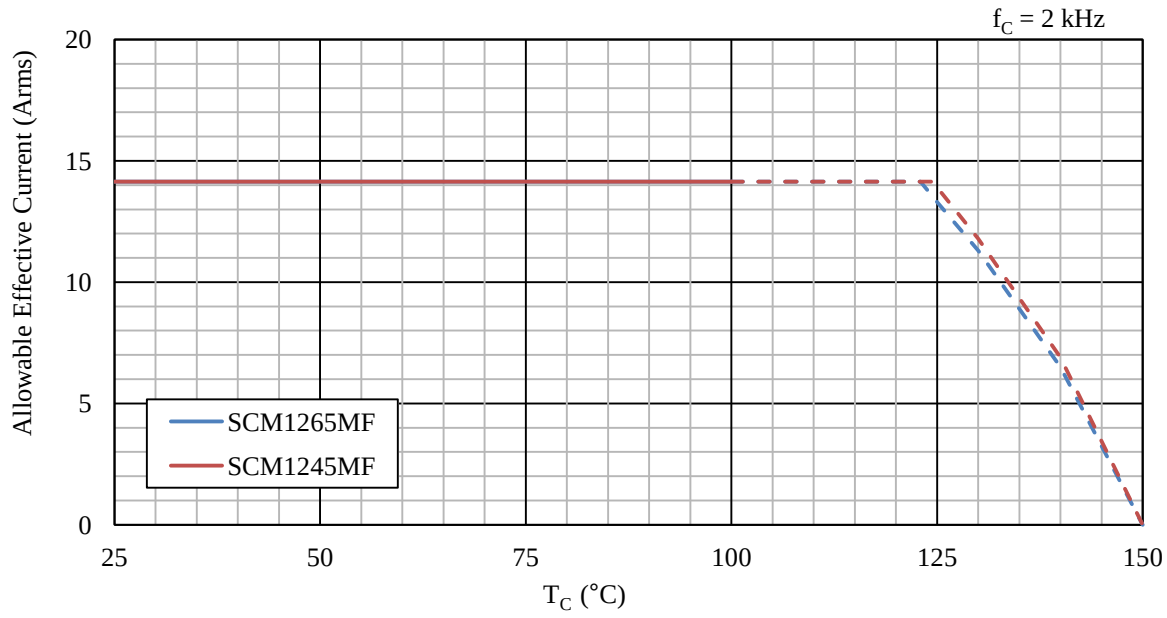


Figure 15-72. Allowable Effective Current (f_C = 2 kHz): 20 A Devices

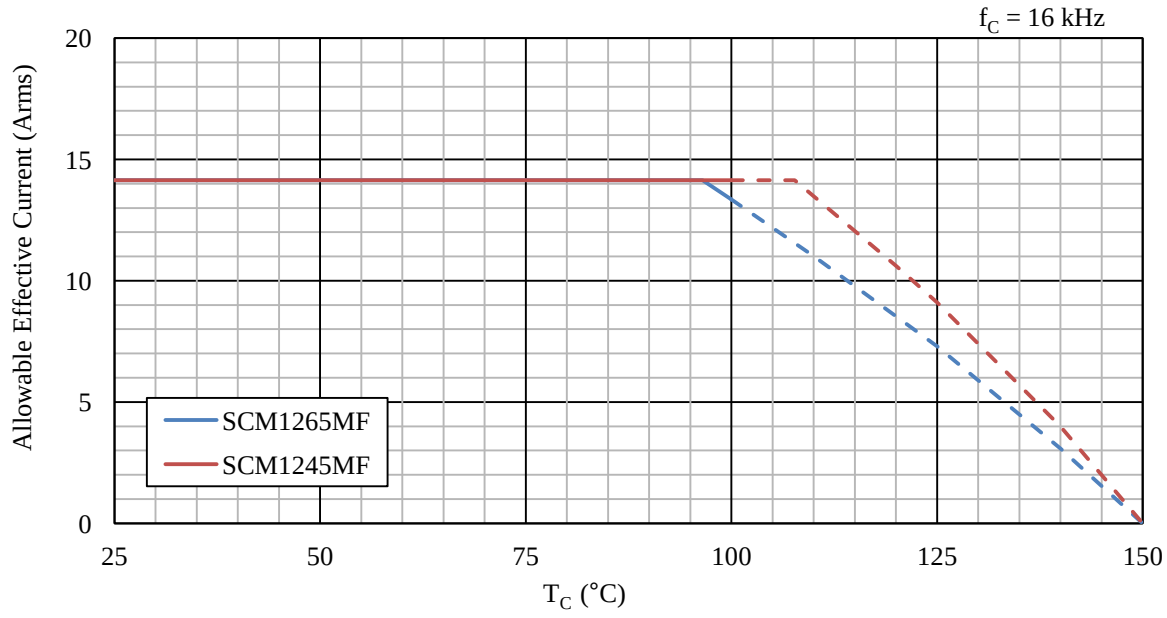


Figure 15-73. Allowable Effective Current (f_C = 16 kHz): 20 A Devices

15.4.4. SCM1256MF, SCM1246MF

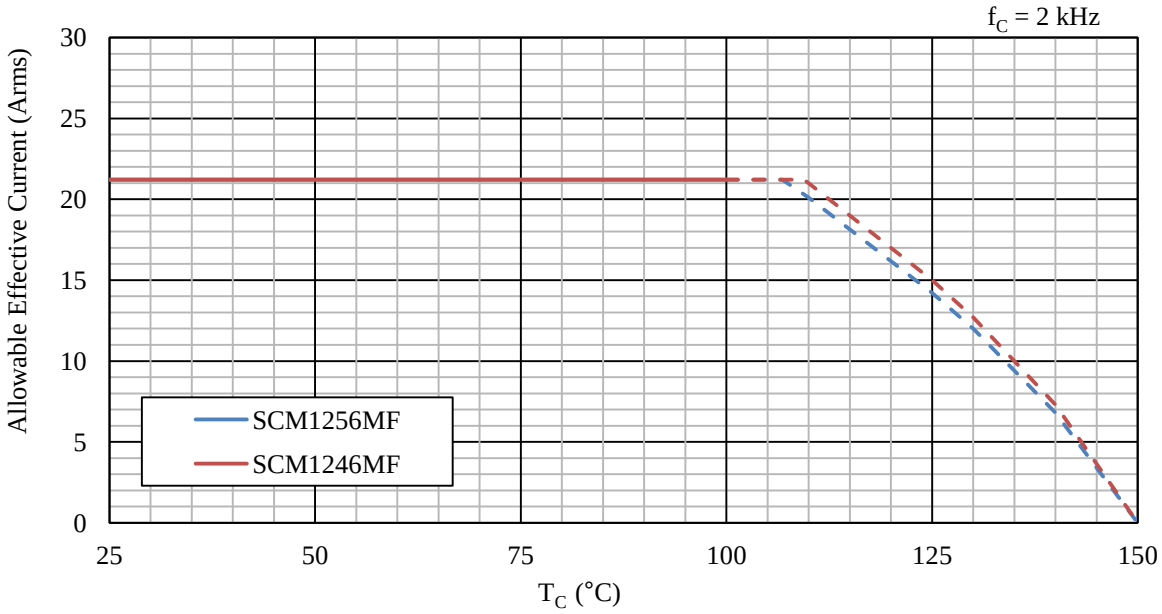


Figure 15-74. Allowable Effective Current (f_C = 2 kHz): 30 A Devices

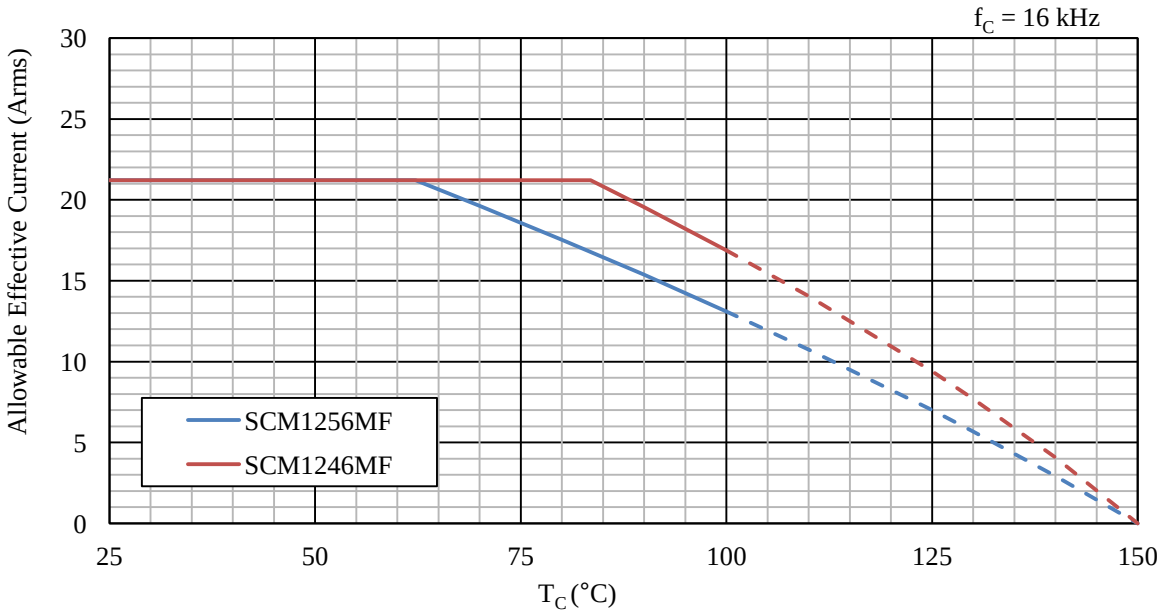
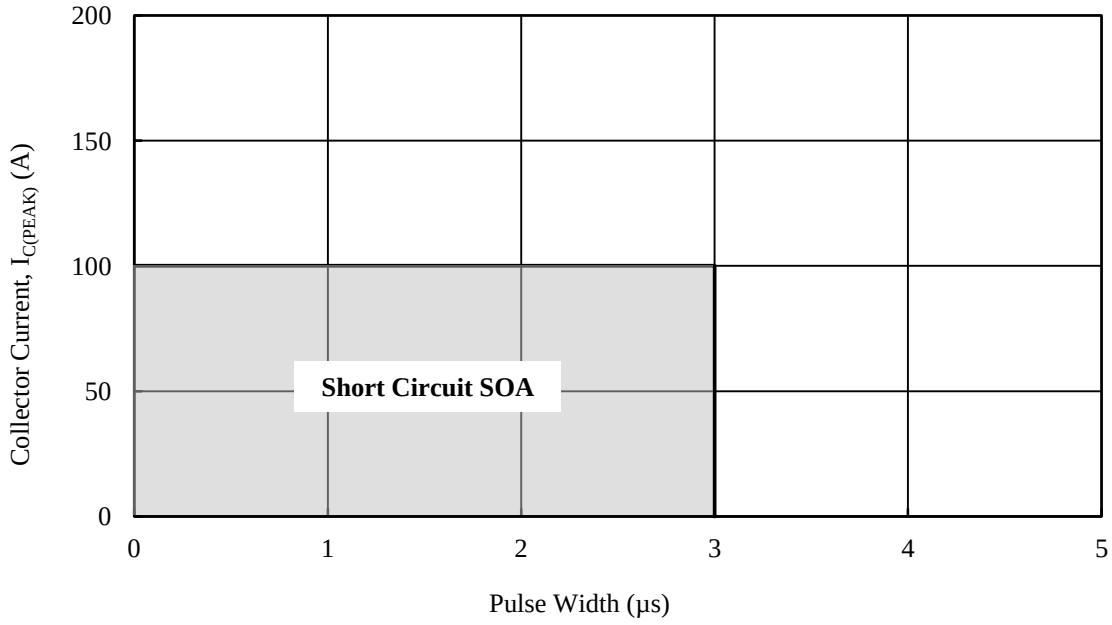


Figure 15-75. Allowable Effective Current (f_C = 16 kHz): 30 A Devices

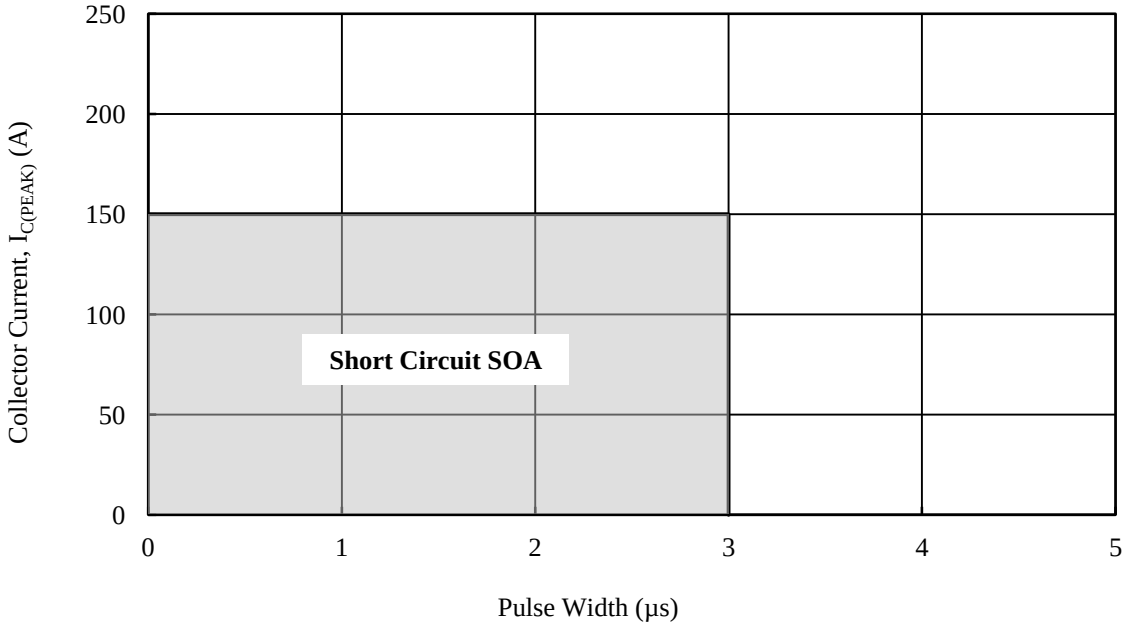
15.5. Short Circuit SOAs (Safe Operating Areas)

Conditions: $V_{DC} \leq 400$ V, $13.5\ V \leq V_{CC} \leq 16.5$ V, $T_j = 125$ °C, 1 pulse.

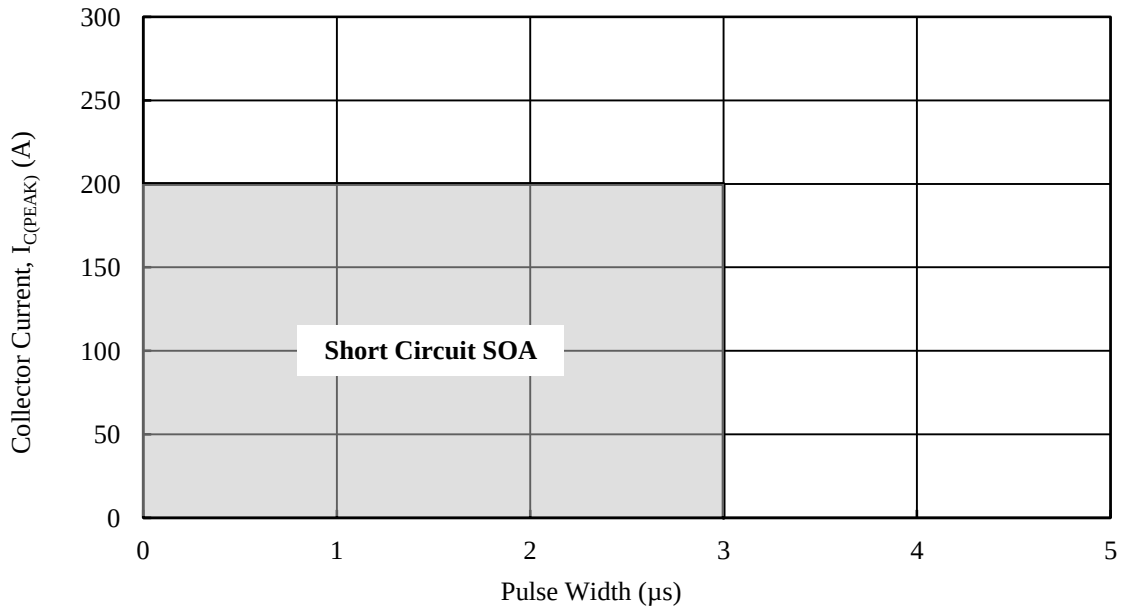
15.5.1. SCM1261MF



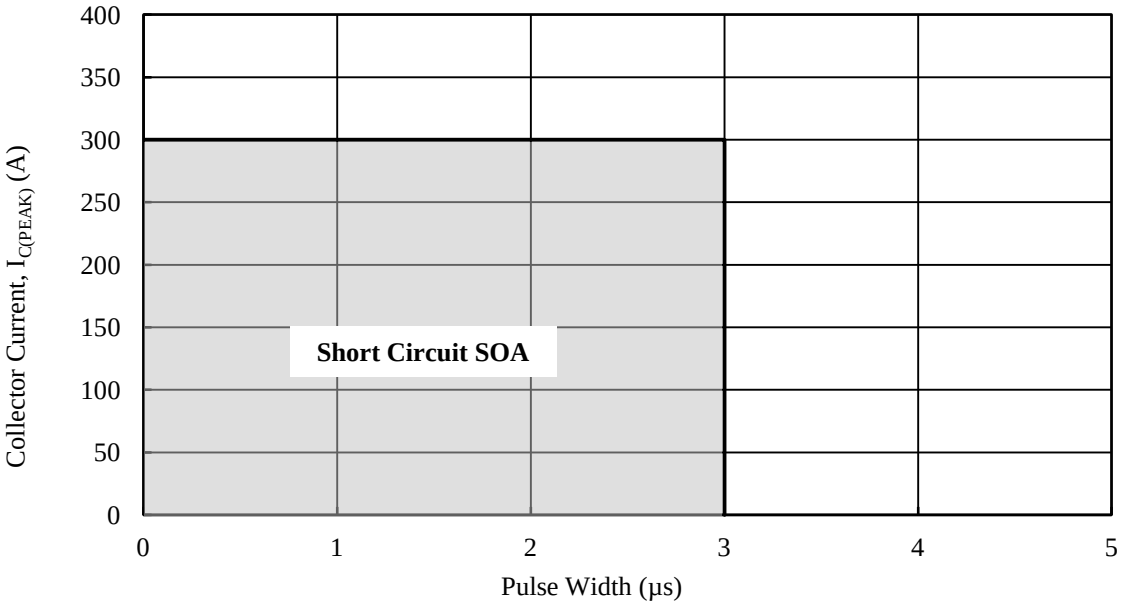
15.5.2. SCM1242MF, SCM1263MF, SCM1243MF



15.5.3. SCM1265MF, SCM1245MF



15.5.4. SCM1256MF, SCM1246MF



16. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SCM1200MF series device. For reference terminal hole sizes, see Section 10.3.

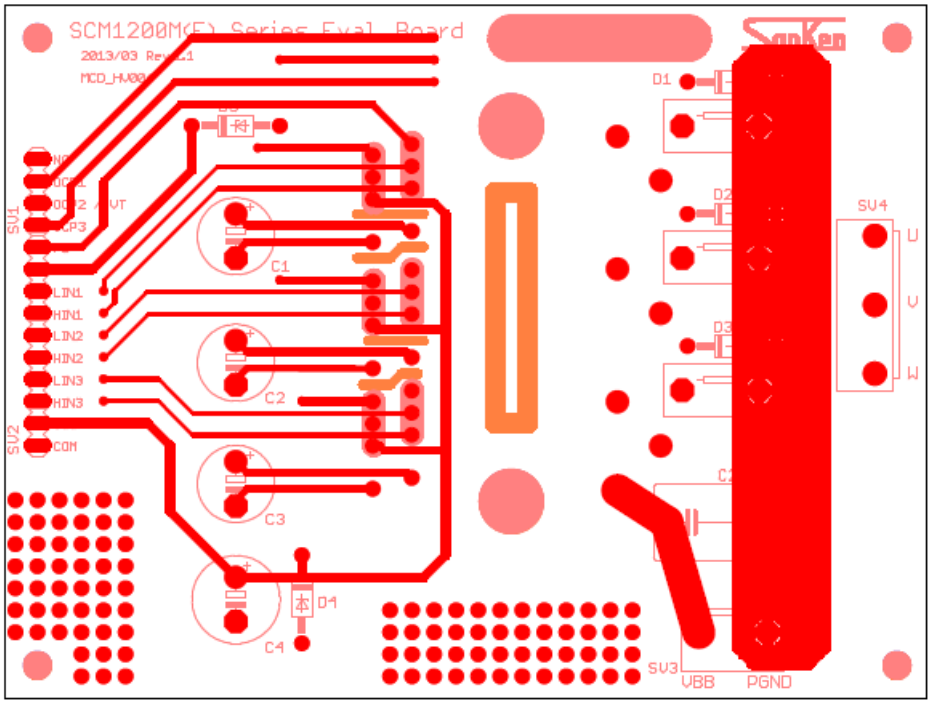


Figure 16-1. Top View

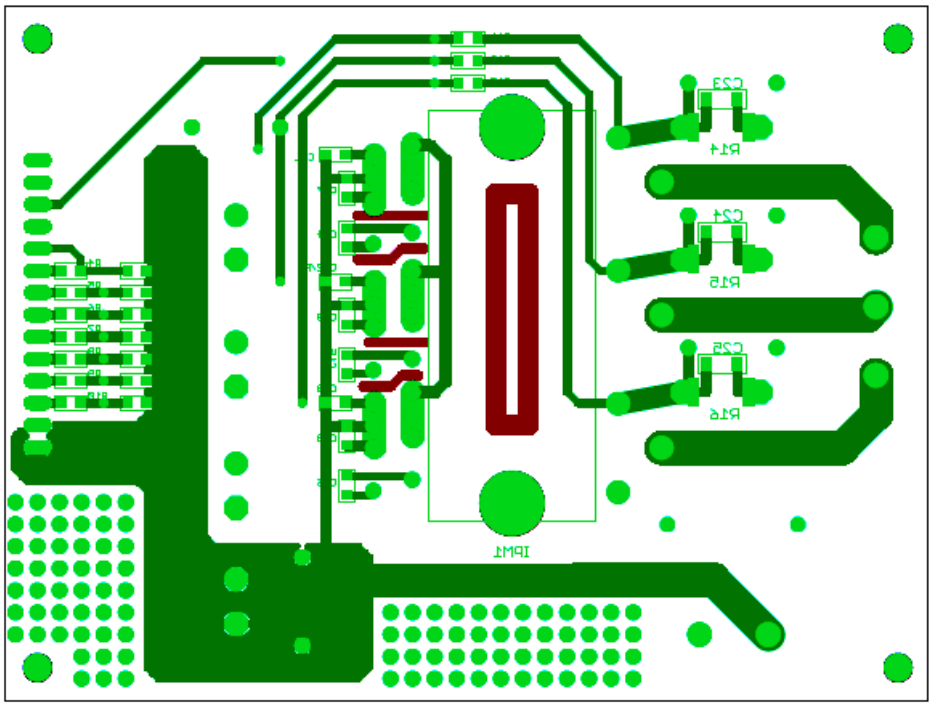


Figure 16-2. Bottom View

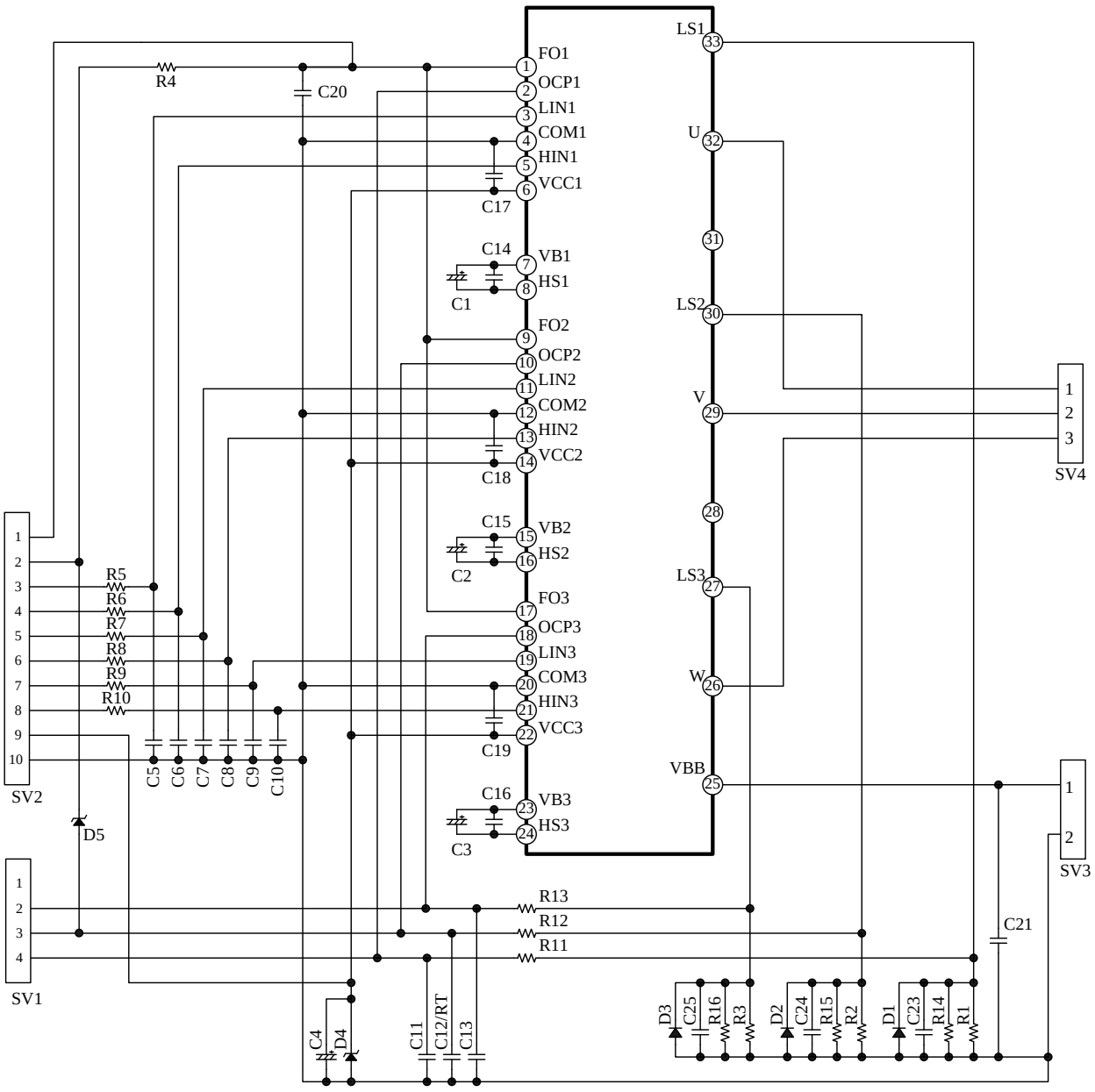


Figure 16-3. Circuit Diagram of PCB Pattern Layout Example

17. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- Motor Driver Specifications

IC	SCM1242MF
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Output Power Rating	1.35 kW

- Circuit Diagram

  See Figure 16-3.

- Bill of Materials

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Electrolytic	47 µF, 50 V	R1*	Metal plate	27 mΩ, 2 W
C2	Electrolytic	47 µF, 50 V	R2*	Metal plate	27 mΩ, 2 W
C3	Electrolytic	47 µF, 50 V	R3*	Metal plate	27 mΩ, 2 W
C4	Electrolytic	100 µF, 50 V	R4	General	4.7 kΩ, 1/8 W
C5	Ceramic	100 pF, 50 V	R5	General	100 Ω, 1/8 W
C6	Ceramic	100 pF, 50 V	R6	General	100 Ω, 1/8 W
C7	Ceramic	100 pF, 50 V	R7	General	100 Ω, 1/8 W
C8	Ceramic	100 pF, 50 V	R8	General	100 Ω, 1/8 W
C9	Ceramic	100 pF, 50 V	R9	General	100 Ω, 1/8 W
C10	Ceramic	100 pF, 50 V	R10	General	100 Ω, 1/8 W
C11	Ceramic	2200 pF, 50 V	R11	General	100 Ω, 1/8 W
C12/RT	Ceramic	2200 pF, 50 V	R12	General	100 Ω, 1/8 W
C13	Ceramic	2200 pF, 50 V	R13	General	100 Ω, 1/8 W
C14	Ceramic	0.1 µF, 50 V	R14*	General	Open
C15	Ceramic	0.1 µF, 50 V	R15*	General	Open
C16	Ceramic	0.1 µF, 50 V	R16*	General	Open
C17	Ceramic	0.1 µF, 50 V	D1	General	1 A, 50 V
C18	Ceramic	0.1 µF, 50 V	D2	General	1 A, 50 V
C19	Ceramic	0.1 µF, 50 V	D3	General	1 A, 50 V
C20	Ceramic	0.01 µF, 50 V	D4	Zener	V_Z = 20 V, 0.5 W
C21	Film	0.1 µF, 630 V	D5	General	Open
C22*	Ceramic	0.1 µF, 50 V	SV1	Pin header	Equiv. to MA04-1
C23*	Ceramic	0.1 µF, 50 V	SV2	Pin header	Equiv. to MA10-1
C24*	Ceramic	0.1 µF, 50 V	SV3	Connector	Equiv. to B2P3-VH
C25	Ceramic	Open	SV4	Connector	Equiv. to B3P5-VH
			IPM1	IC	SCM1242MF

* Refers to a part that requires adjustment based on operation performance in an actual application.

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